

RC Snubber for Class-D Audio Amplifiers

INTRODUCTION

High speed switching of power MOSFETs in the power stage of Class-D amplifiers results in output voltage over/undershoot and high frequency ringing on the output waveform, as shown in Figure 1.

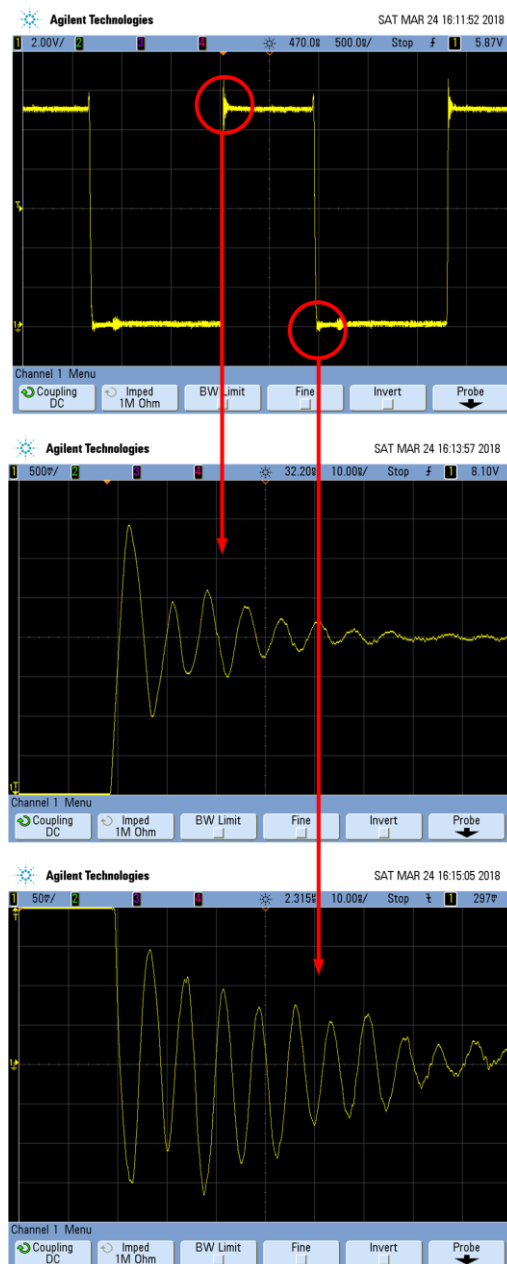


Figure 1 Class-D output over/undershoot and ringing

The over/undershoot places additional stress on the power MOSFETs, potentially reducing MOSFET lifetime or, in extreme cases, causing avalanche breakdown.

The high frequency ringing can couple to nearby PCB planes and cables and is therefore a source of radiated emissions (see Reference 1). Radiated emissions can be particularly problematic in portable electronics where the Class-D amplifier may be some distance from the micro speaker and connected by a relatively long unshielded twisted pair or flex cable.

An LC filter on the output of the Class-D amplifier can be used to attenuate the ringing, reducing radiated emissions. However, this does not reduce the voltage stress on the power MOSFETs.

This application note describes the cause of the over/undershoot and high frequency ringing and details the design of an RC network to damp the ringing at source, to reduce voltage stress and radiated emissions.

CAUSE OF OVER/UNDERSHOOT AND HIGH FREQUENCY RINGING

Class-D amplifiers for portable electronics are invariably full-bridge architectures to maximize signal swing and therefore output power. For simplicity Figure 2 shows one half of the full bridge power stage. The diagram shows n/p-channel power MOSFETs, pre-drivers, and supply rail decoupling capacitor.

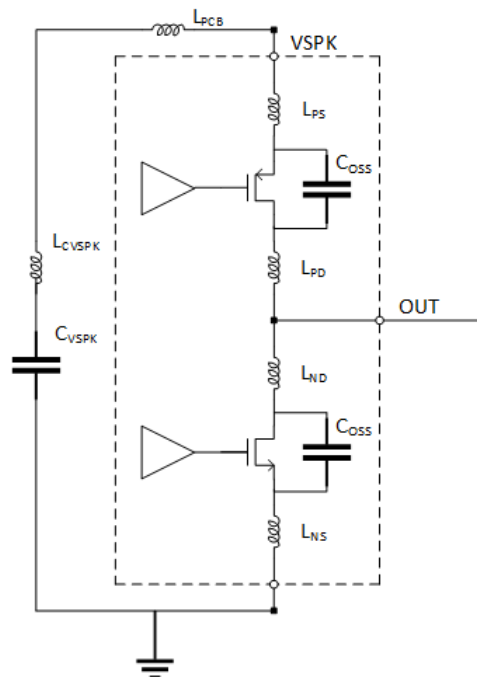


Figure 2 Class-D power stage with parasitic components

Figure 2 also shows parasitic components, including supply rail decoupling capacitor ESL (L_{CVSPK}), PCB trace inductance (L_{PCB}), IC package/routing inductance in the source and drain of power MOSFETs (L_{PS} , L_{PD} , L_{ND} , L_{NS}), and power MOSFET output capacitance in parallel with stray package and PCB capacitance (C_{OSS}). These parasitic components are the cause of over/undershoot and high frequency ringing (see Reference 2).

When the n-channel power MOSFET switches off, there is a short dead time where the n-channel power MOSFET body diode conducts. The rising-edge ringing occurs when the p-channel power MOSFET turns on and the n-channel body diode turns off. The n-channel power MOSFET total parallel parasitic capacitance is charged through the parasitic inductances. This LC tank is the cause of overshoot and high frequency ringing.

The frequency of ringing at turn on of p-channel power MOSFET is determined by the n-channel power MOSFET output capacitance (C_{OSS}) and the total inductance of the current loop ($L_{CVSPK} + L_{PCB} + L_{PS} + L_{PD} + L_{ND} + L_{NS}$). The energy dissipates in the on-resistance of the p-channel power MOSFET and so the ringing decays over several cycles.

Similarly, when the p-channel power MOSFET turns off, the n-channel power MOSFET body diode turns on due to flyback of the speaker inductance. The p-channel power MOSFET output capacitance is charged through the total loop inductance causing under-shoot and high frequency ringing.

RC SNUBBER DESIGN

Ringing can be almost eliminated (snubbed) by an RC network on the output of the Class-D amplifier as shown in Figure 3. R_{SN} and C_{SN} damp the voltage over/undershoot and ringing.

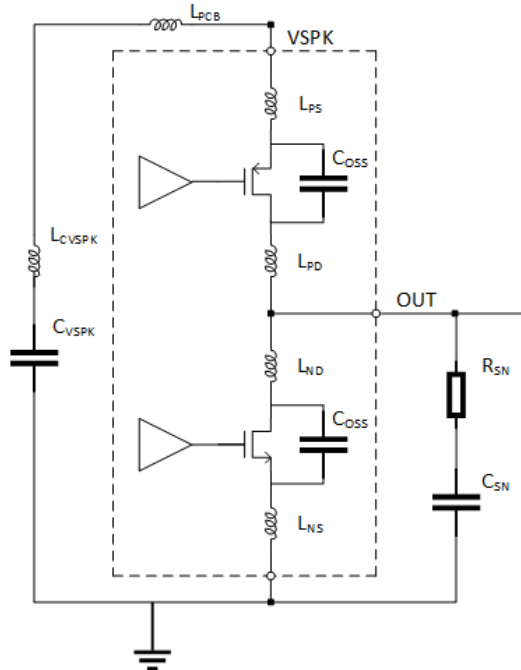


Figure 3 Class-D power stage with RC snubber

Adding an RC snubber damps out ringing, at the expense of increased switching losses.

The snubber should be connected directly across the drain and source of the n-channel power MOSFET.

The values for the power MOSFET output capacitance and IC package inductance are not always available from IC vendors. Similarly, capacitor package ESL is not readily available. Measuring the parasitic inductance and capacitance directly is difficult due to the small non-linear values and PCB parasitic effects change from application to application.

So, snubber design is typically based on empirical measurements. Snubber component placements are included on the PCB layout and bench measurements are used to extract the value of parasitic capacitance and inductance. Snubber resistor and capacitor values can then be calculated, and the RC snubber populated.

The procedure below (see Reference 3) uses bench measurements to design the RC snubber circuit, while a more rigorous discussion of snubber design is outlined in Reference 4.

DETERMINING PARASITIC CAPACITANCE AND INDUCTANCE

The resonant frequency, f_0 , of the parasitic LC circuit is given by Equation 1:

$$f_0 = \frac{1}{2\pi\sqrt{L_p C_{OSS}}} \quad (1)$$

Where L_p is the equivalent parasitic inductance and C_{OSS} is the n-channel power MOSFET total parallel parasitic capacitance.

If an external capacitor, C_{EXT} , is placed between OUT and ground, a different resonant frequency, f_1 , can be observed, and C_{OSS} can be calculated as follows:

$$C_{OSS} = \frac{C_{EXT}}{\chi^2 - 1} \quad (2)$$

Where:

$$\chi = \frac{f_0}{f_1} \quad (3)$$

Once C_{OSS} is known L_p can be calculated from Equation 1:

$$L_p = \frac{1}{(2\pi f_0)^2 C_{OSS}} \quad (4)$$

CALCULATING SNUBBER RESISTOR VALUE

Once the parasitic capacitance and inductance are known, the snubber damping resistor value can be calculated.

The damping factor of a parallel RLC circuit is given by:

$$\zeta = \frac{1}{2R_{SN}} \sqrt{\frac{L_p}{C_{OSS}}} \quad (5)$$

A damping factor of 1 (critically damped) is chosen for fastest possible rise time with no overshoot (see Reference 5). So, rearranging Equation 5 for R_{SN} :

$$R_{SN} = \frac{1}{2} \sqrt{\frac{L_p}{C_{OSS}}} \quad (6)$$

SNUBBER CAPACITOR VALUE

A good choice of snubber capacitor, C_{SN} , for effective damping and to minimize resistor power loss is $3 \times C_{OSS}$ (see Reference 4).

The average power dissipated in the snubber resistor is calculated as shown in Equation 7 (see Reference 6).

$$P_{RSN} = C_{SN} V_{SPK}^2 f_{SW} \quad (7)$$

The snubber resistor must have a suitable power rating and is chosen based on corporate derating guidelines.

EXAMPLE SNUBBER DESIGN

Figure 4 shows CS35L41 boosted Class-D amplifier output voltage overshoot and ringing. The waveform shows the unsnubbed ringing frequency is 111.11 MHz

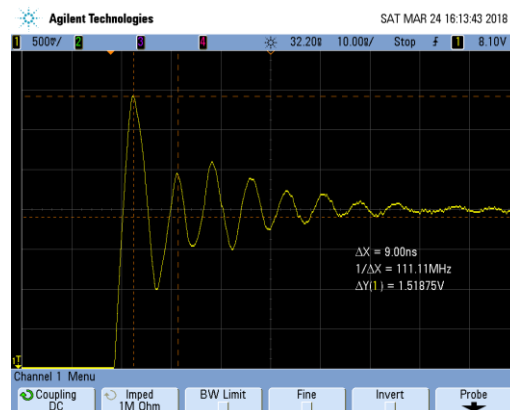


Figure 4 CS35L41 output voltage overshoot and ringing

An external 1 nF capacitor is added to the output and a new ringing frequency of 45.87 MHz is observed, as shown in Figure 5.

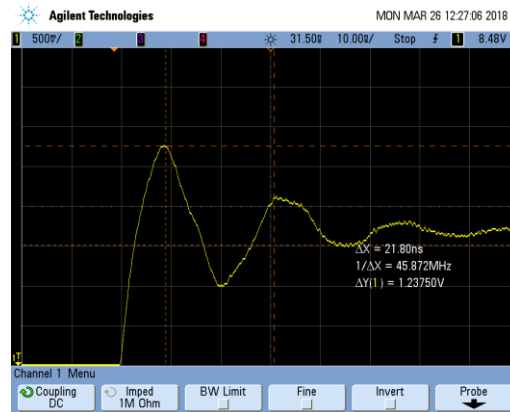


Figure 5 CS35L41 output voltage overshoot and ringing with 1 nF external capacitor

The n-channel power MOSFET output capacitance is calculated as shown in Equation 2:

$$C_{oss} = \frac{1nF}{\left(\frac{111.11MHz}{45.87MHz}\right)^2 - 1} = 205.45 pF$$

Total parasitic inductance is then calculated using Equation 4:

$$L_p = \frac{1}{(2\pi 111.11MHz)^2 205.45pF} = 9.99 nH$$

Snubber resistor is calculated using Equation 6:

$$R_{SN} = \frac{1}{2} \sqrt{\frac{9.99nH}{205.45pF}} = 3.45 \Omega$$

Preferred component value 3Ω is chosen for snubber resistor and 560 pF for snubber capacitor (approximately 3 x C_{oss}). For best performance, a COG/NP0 ceramic capacitor is recommended.

Average power consumption of the snubber resistor is calculated using Equation 7:

$$P_{RSN} = 560pF \times 11^2 \times 430KHz = 29 mW$$

Figure 6 shows the high frequency ringing has been significantly damped by the snubber. The overshoot amplitude is approximately 3 times smaller, and the ringing dies out after only a few oscillations.

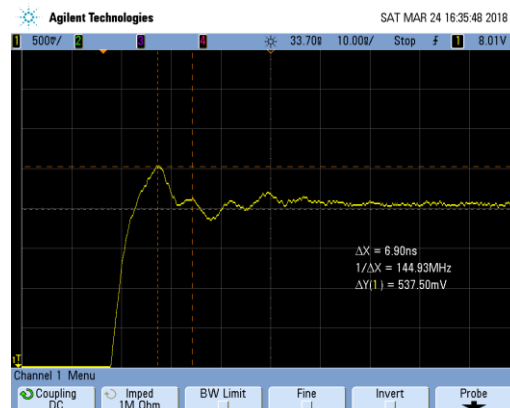


Figure 6 CS35L41 output voltage with RC snubber

The common-mode spectrum of the PCB traces connecting Class-D amplifier CS35L41 to an 8 Ω , 33 μ H load is measured in accordance with IEC 61967-4 (see Reference 7) using Rohde & Schwarz ESRP7 EMI test receiver. Figure 7 shows that with the RC snubber there is approximately 12 dBm attenuation at the ringing frequency.

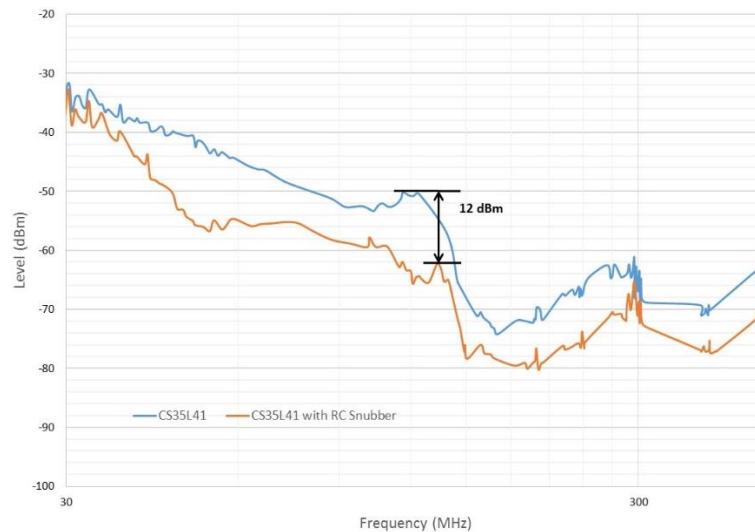


Figure 7 CS35L41 common-mode spectrum

CONCLUSIONS

Voltage over/undershoot and ringing on the outputs of Class-D amplifiers can cause additional stress to the power MOSFETs and lead to unacceptable radiated emissions.

An LC filter on the outputs attenuates radiated emissions but does not reduce voltage stress.

Over/undershoot and high frequency ringing is caused by resonances in parasitic inductance and capacitance.

An RC snubber across the low-side Class-D power MOSFET can effectively damp the parasitic LC tank.

Empirical measurements and straightforward calculations can be used to design the snubber circuit.

REFERENCES

- [1] Keong W. Kam, David Pommerenke, Cheung-Wei Lam, Robert Steinfeld, EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis, IEEE International Symposium on Electromagnetic Compatibility, 2008
- [2] T. Tolle, T. Duerbaum, R. Elferich, Switching Loss Contributions of Synchronous Rectifiers in VRM applications, Power Electronics Specialist Conference, 2003
- [3] NXP Semiconductors, AN11160 Designing RC snubbers, 2012
- [4] Rudy Severns, Snubber Circuits For Power Electronics, 2008
- [5] Christophe Basso, The Link Between The Phase Margin And The Converter Transient Response
- [6] International Rectifier, Class D Amplifier Design Basics II, 2009
- [7] IEC 61967-4 Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 4: Measurement of conducted emissions, 1 ohm/150 ohm direct coupling method

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to www.cirrus.com.

The products and services of Cirrus Logic International (UK) Limited; Cirrus Logic, Inc.; and other companies in the Cirrus Logic group (collectively either "Cirrus Logic" or "Cirrus") are sold subject to Cirrus Logic's terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. Software is provided pursuant to applicable license terms. Cirrus Logic reserves the right to make changes to its products and specifications or to discontinue any product or service without notice. Customers should therefore obtain the latest version of relevant information from Cirrus Logic to verify that the information is current and complete. Testing and other quality control techniques are utilized to the extent Cirrus Logic deems necessary. Specific testing of all parameters of each device is not necessarily performed. In order to minimize risks associated with customer applications, the customer must use adequate design and operating safeguards to minimize inherent or procedural hazards. Cirrus Logic is not liable for applications assistance or customer product design. The customer is solely responsible for its product design, including the specific manner in which it uses Cirrus Logic components, and certain uses or product designs may require an intellectual property license from a third party. Features and operations described herein are for illustrative purposes only and do not constitute a suggestion or instruction to adopt a particular product design or a particular mode of operation for a Cirrus Logic component.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS LOGIC PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, NUCLEAR SYSTEMS, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS LOGIC PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS LOGIC DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS LOGIC PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS LOGIC PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS LOGIC, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

This document is the property of Cirrus Logic, and you may not use this document in connection with any legal analysis concerning Cirrus Logic products described herein. No license to any technology or intellectual property right of Cirrus Logic or any third party is granted herein, including but not limited to any patent right, copyright, mask work right, or other intellectual property rights. Any provision or publication of any third party's products or services does not constitute Cirrus Logic's approval, license, warranty or endorsement thereof. Cirrus Logic gives consent for copies to be made of the information contained herein only for use within your organization with respect to Cirrus Logic integrated circuits or other products of Cirrus Logic, and only if the reproduction is without alteration and is accompanied by all associated copyright, proprietary and other notices and conditions (including this notice). This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale. This document and its information is provided "AS IS" without warranty of any kind (express or implied). All statutory warranties and conditions are excluded to the fullest extent possible. No responsibility is assumed by Cirrus Logic for the use of information herein, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. Cirrus Logic, Cirrus, the Cirrus Logic logo design, and SoundClear are among the trademarks of Cirrus Logic. Other brand and product names may be trademarks or service marks of their respective owners.

Copyright © 2018 Cirrus Logic, Inc. All rights reserved.

REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
MAR '18	1	Initial release	-	Terence Orr