AN306

Simplifying System Design Using the CS4350 PLL DAC

1. INTRODUCTION

Typical Digital to Analog Converters (DACs) require a high-speed Master Clock to clock their digital filters and modulators, as well as some portions of their discrete time analog circuitry. This Master Clock (or system clock) is typically required to be synchronous to the left-right (frame or word) clock (LRCK) in order to maintain sample alignment in the digital filters, state machines, modulator and discrete time analog sections. Figure 1 below shows an example of a typical DAC clocked by an external Master Clock. The clock is applied to the MCLK pin and then distributed to any internal logic that requires it.

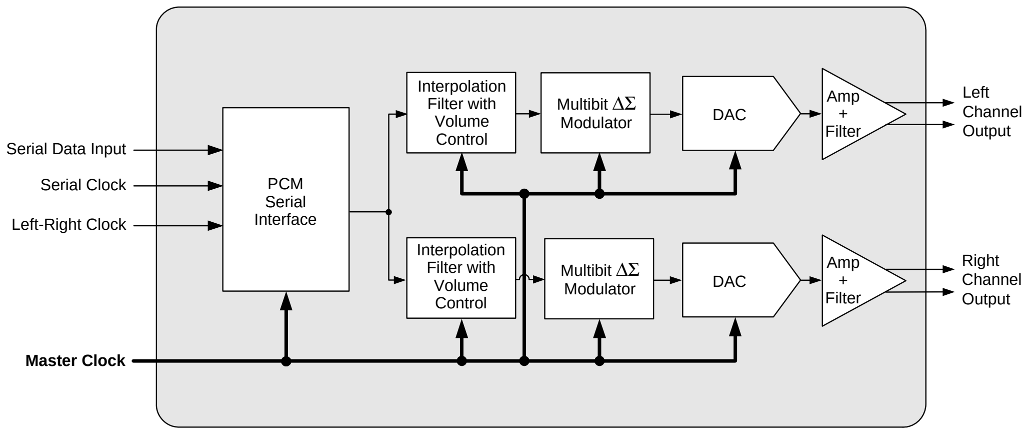

Figure 1. Typical DAC Architecture with Master Clock Input

As an alternative, PLL DACs are designed to derive their internal synchronous Master Clock from some other external source. This source could be any clock, but in practice it is commonly a video clock (27 MHz) or one of the slower SCLK or LRCK signals which are mandatory for typical PCM audio interfaces (See AN282 “The 2-Channel Serial Audio Interface: A Tutorial”). In practice, the CS4350 PLL DAC generates its Master Clock from the input left-right clock. Figure 2 shows the CS4350 PLL DAC architecture; from the input LRCK signal, the internal PLL derives the Master Clock signal that is used to drive the internal system timing.

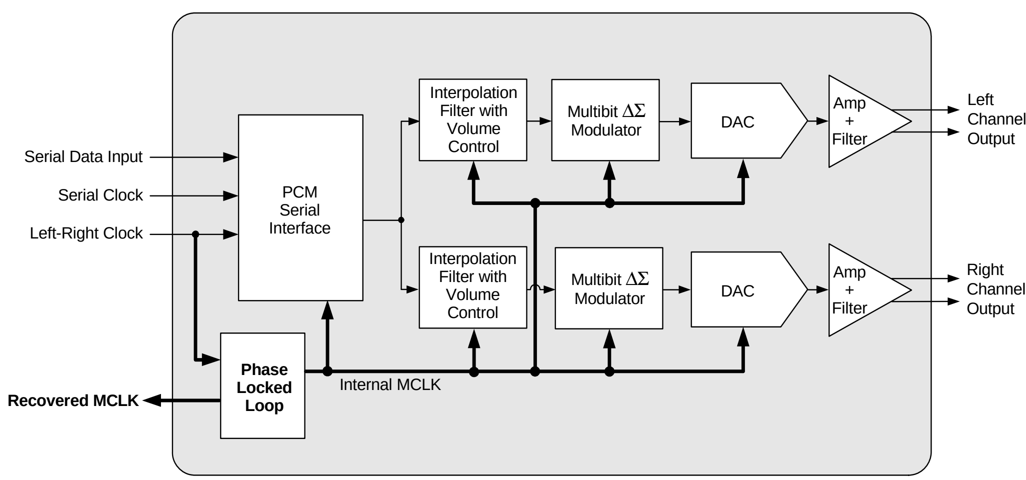

Figure 2. CS4350 PLL DAC Architecture

The internal Master Clock generation of a PLL DAC yields inherent benefits that simplify the design of audio systems. The CS4350’s unique implementation of the feature takes the concept a step further to provide an even greater degree of design simplicity, flexibility, and performance.

2. SIMPLIFIED SYSTEM DESIGN

In the design and layout of an audio mixed signal system, the conditioning and routing of the clocks are one of the most important considerations. Because a converter's Master Clock signal provides the sample clock that is used as the time base for its modulator and switched analog filters, it is typically the most sensitive to jitter and clock coupling. Eliminating the need for an external Master Clock signal provides for easier signal routing, reduced potential for electromagnetic interference (EMI), and improved jitter immunity.

2.1 Eased Signal Routing

The Master Clock is typically generated in the digital section of a mixed signal system. This high-speed clock then needs to be routed across the board to the analog or mixed signal section in order to provide the master clock for the converters. Since the CS4350 PLL DAC does not require a Master Clock input signal, it does not need to be routed across the system board to reach the converter. This eases the routing necessary for the remaining clocks.

2.2 Reduced Potential for EMI

The Master Clock is typically the fastest clock used by a mixed signal audio converter. Routing any high-speed clock takes careful consideration in order to keep EMI to a minimum. The CS4350 PLL DAC provides an easy way to ease EMI concerns by removing the dependency on the Master Clock, thus reducing the number of high-speed clocks necessary to implement an audio subsystem.

2.3 Improved Jitter Immunity

As system designs become increasingly complex, the system clocking sources also become increasingly complex. In many designs, the system clock is derived from a PLL within a large SOC (System on a Chip), and is often used as the Master Clock source for the audio converters. The clocks generated from such SOCs often exhibit high amounts of jitter, primarily as a result of the many asynchronous operations within the SOC coupling into the clock signal. This high amount of jitter often limits the distortion (THD+N) performance and dynamic range of the mixed signal systems that use the SOC generated system clock.

Because the CS4350 PLL DAC generates its Master Clock internally, the jitter on an SOC or other system clock source is of no consequence. When locking to LRCK, the CS4350's PLL can reject any high-frequency jitter that may be present on the slower LRCK.

3. LOCKING TO LRCK

The CS4350's PLL locks to the incoming LRCK signal, and locking to LRCK provides some noteworthy advantages over locking to another clock in the system. Specifically, locking to a system or video clock requires routing a high-speed clock to the converter and does not provide the EMI and routing advantages of locking to LRCK. Locking to LRCK also provides for improved jitter rejection due to the lower native frequency of the left-right clock; this allows a lower high-pass corner to be achieved in the PLL's loop filter. When locking to LRCK, no other clocks are needed beyond those already required in the serial PCM interface (SCLK, LRCK, and SDATA).

4. NO EXTERNAL LOOP FILTER COMPONENTS

A typical PLL consists of a phase comparator, charge pump, loop filter and a VCO. The loop filter creates an analog filter for the internal VCO control signal. Many PLLs require the loop filter components (typically two capacitors and a resistor) to be external to the device because of internal size constraints. The CS4350 PLL uses a PLL configuration that requires no external PLL loop filter components. This allows the converter's PLL to be self-sufficient and also reduces the implementation cost in terms of external component price and total integration area.

5. LOCALIZED MASTER CLOCK RECOVERY AND DISTRIBUTION

The Recovered Master Clock (RMCK) output is a unique feature of the CS4350. The RMCK output allows the CS4350's high-speed recovered clock Master Clock signal to be used as the Master Clock for other more typical audio converters that do not have built-in PLLs. This feature is useful for localizing the high-speed clock to a portion of the circuit board separate from the rest of the system, or when the integrity of a long Master Clock run could affect the converter performance.

Figure 3 shows the CS4350 receiving only the necessary PCM clocks from a distant source while generating a recovered Master Clock to be used locally to the CS4350. This allows the RMCK signal recovered and provided by the CS4350 to be used in a small area, thereby easing the system design and the routing of clocks.

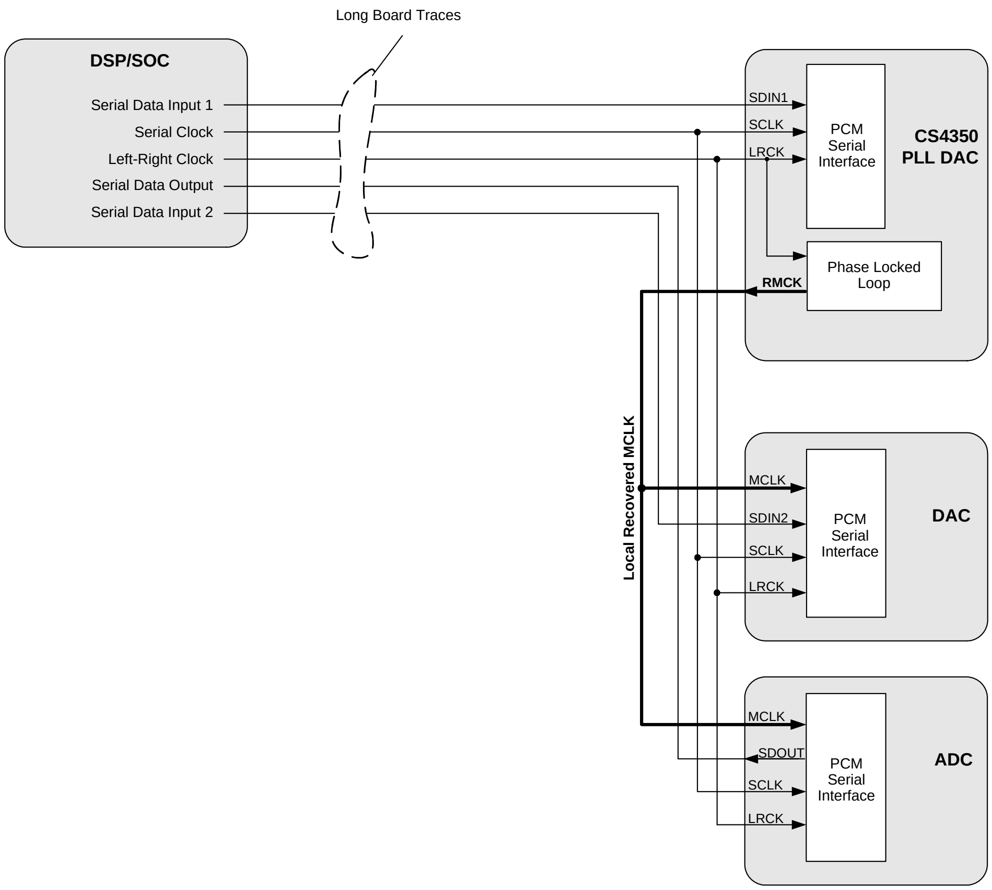

Figure 3. Localized MCLK using CS4350 RMCK Output

Some audio converters require specific MCLK to LRCK ratios that vary according to the sample rate. The CS4350's RMCK output can provide this ratio variance independently from its internal Master Clock signal. This allows flexibility in the local audio converters that are using the CS4350's RMCK output by providing a wider range of MCLK/LRCK ratios for use.

For converters that have an automatic speed mode detection feature, no register writes are necessary to change from 44.1 kHz to 96 kHz sample rates as the CS4350's RMCK can be set to automatically adjust the MCLK to LRCK ratio accordingly. See Section 4.2.1 of the CS4350 data sheet for more details on this feature.

6. OUT-OF-BAND PERFORMANCE

Converters that rely on an external Master Clock signal are often only able to operate with an internal over-sampling rate of 128 times the sample rate (128 x Fs). This can limit the performance of the modulator by requiring the modulator noise shaping to begin rising at a lower frequency than would be possible if a higher modulator rate were available.

Because the CS4350's circuitry has access to the internal high-frequency output of the PLL, it is able to achieve a 4x higher modulator rate than typical audio converters. This allows for much lower out-of-band noise than is typically achievable in a 128x over-sampling DAC. See Figure 4 and Figure 5.

As a result, the CS4350 is able to achieve lower noise within much wider frequency band than many similar typical DACs that require an external Master Clock signal. This can provide significant benefits for applications that are sensitive to noise outside of the typical 20 kHz audio band. Achieving similar out-of-band performance using a typical 128x over-sampling DAC would require high-order off-chip analog filtering.

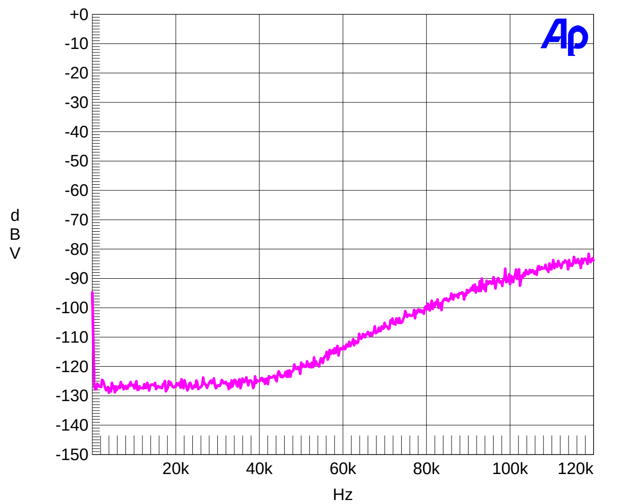

Figure 4. Typical 128x DAC Out-of-Band Noise

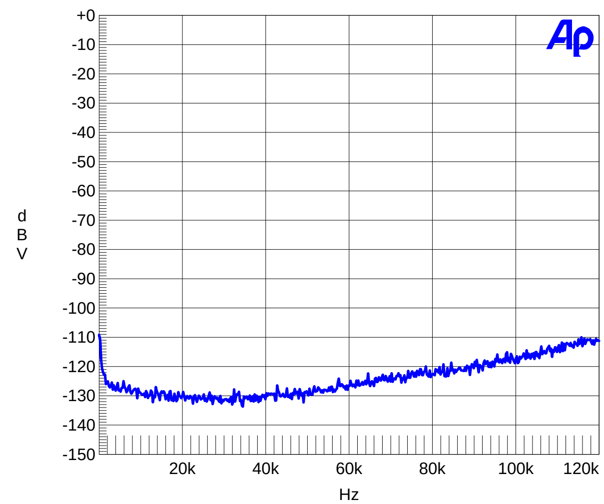

Figure 5. CS4350 Out-of-Band Noise

7. CS4350 ANALOG ARCHITECTURE

The CS4350 implements a current-based DAC with on chip current-to-voltage (I-to-V) conversion and a continuous time summing amplifier. It offers both differential and single-ended analog output options with an analog supply of 3.3 V or 5 V. For design flexibility, the full-scale output reference level is set by an internal fixed reference to allow operation with a 2 Vrms differential, or 1 Vrms single-ended output, regardless of changes to the VA supply.

8. CONCLUSIONS

The CS4350 PLL DAC offers a number of advantages relative to conventional digital-to-analog converters, each of which can be instrumental in simplifying the design of audio systems. From flexible output options, to localized Master Clock recovery and distribution, to low out-of-band noise performance, to system clock jitter independence, to the easing of PCB layout and EMI concerns, the CS4350 can be called upon to solve many real-world problems of audio system designers.

For more information about the CS4350 PLL DAC, please refer to the CS4350 datasheet available at www.cirrus.com.

REVISION HISTORY

Revision	Changes
REV1	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.