

Load Cell Measurement using the CS3001/02/11/12 Amplifiers with the CS5510/11/12/13 ADCs

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1. INTRODUCTION

Several circuits will be presented that use the CS3001/02/11/12 operational amplifiers with the CS5510/11/12/13 ADCs. The combination yields very high performance at relatively low power.

2. CS3001 AND CS5513 COMBINATION CIRCUIT

The first circuit illustrates the CS3001 single amplifier with the CS5513 A/D converter. The CS5513 converter includes an internal oscillator that sets the conversion rate at approximately 107 Sps.

In this circuit the load cell sensitivity is 1 mV / V. With 5 V excitation and full load, the output from the load cell will be 5 mV.

The CS3001 amplifier is a chopper-stabilized amplifier with very low noise ($6 \text{ nV} / \sqrt{\text{Hz}}$). The amplifier is unique in that it has 300 dB of open loop gain. This permits the amplifier to be used in very-high-gain configurations and still maintain excellent linearity.

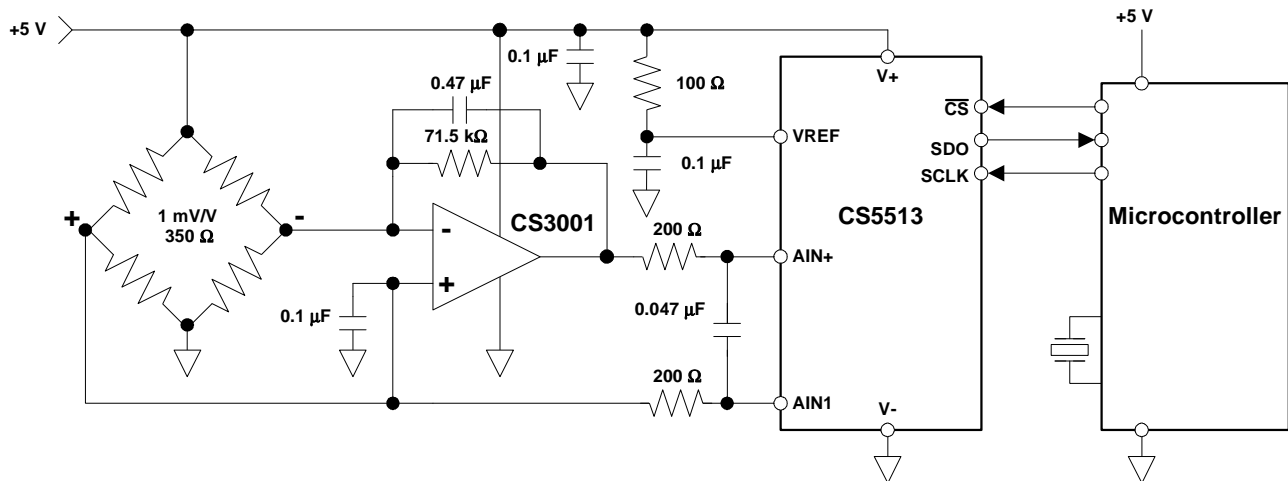


Figure 1.

The circuit shows the CS3001 set with a gain of 408X. The gain is set by the ratio of the feedback resistor (71.5 k) and the output resistance of the load cell (175 ohm which is set by the parallel combination of the two 350-ohm resistors inside the bridge). Note that few op amps can support a gain of 408x (52 dB) and guarantee 16-bit or better linearity; the CS3001 will be 20-bit linear due to its super-high open-loop gain. Note that the amplifier output is referenced to the common mode voltage of the load cell at about one half the supply, or 2.5 V. The 5 mV output of the load cell is amplified by the op amp gain of 408 to yield an input to the ADC of 2.04 V, but this will be on top of the 2.5 volt common mode signal. The combination will result in a signal of about 4.504 volts on the AIN+ input of the ADC.

The input span of the ADC is set by the VREF voltage. With 5 V into VREF, the span of the converter is set to approximately $\pm 4 \text{ V}$, fully differential. The CS5513 is a 20-bit converter so its transfer function of 1,048,576 codes is across 8 Vpp. Since the amplified load cell signal is only 2.04 volts the converter will output only about one quarter

of the codes ($[(2.04 / 8) \cdot 1048576] = 267387$) of the converter as the load on the load cell goes from zero to full scale.

But how many of these codes are really usable, since there is noise in the system? Using the specifications for the various elements of the circuit, an estimate of the performance of the system can be derived. The means by which the estimate is derived will be presented and then the circuit will be tested to confirm that the derivation is valid.

The op amp is configured for the inverting gain configuration. The positive terminal of the bridge is connected to the positive terminal of the op amp to establish the common mode voltage for the op amp as an inverting amplifier. The effective resistance of each of the output terminals of the bridge is about 175 ohms each (two 350 ohm resistors in parallel). The spot noise of this resistance is about $1.7 \text{ nV} / \sqrt{\text{Hz}}$. The op amp spot noise is $6 \text{ nV} / \sqrt{\text{Hz}}$. The amount of noise ($33.8 \text{ nV} / \sqrt{\text{Hz}}$) from the 71.5 k Ω resistor will be divided down by $175 / (71500 + 175)$ to become $0.08 \text{ nV} / \sqrt{\text{Hz}}$ at the input of the op amp. If these noise sources are summed in rms fashion, the result is $\sqrt{(1.7^2 + 1.7^2 + 0.08^2 + 6^2)} = 6.46 \text{ nV} / \sqrt{\text{Hz}}$. It is apparent that the op amp is the dominate source of noise. The effect of the noise of the ADC has not been included at this point. The amplifier will amplify the noise at its input by the noise gain of the amplifier which is 409 (noise gain of an inverting amplifier is $1 +$ its forward gain of 408). But the bandwidth is limited by the 0.47 μF and the 71.5K due to its 4.73 Hz corner frequency. This analysis will ignore the fact that the capacitor may be $\pm 20\%$ tolerance. So the op amp noise referred to the input of the ADC will be about $6.46 \text{ nV} / \sqrt{\text{Hz}} \cdot 409 = 2642 \text{ nV} / \sqrt{\text{Hz}}$ or 2.642 microvolts / $\sqrt{\text{Hz}}$ across the noise bandwidth of the analog filter.

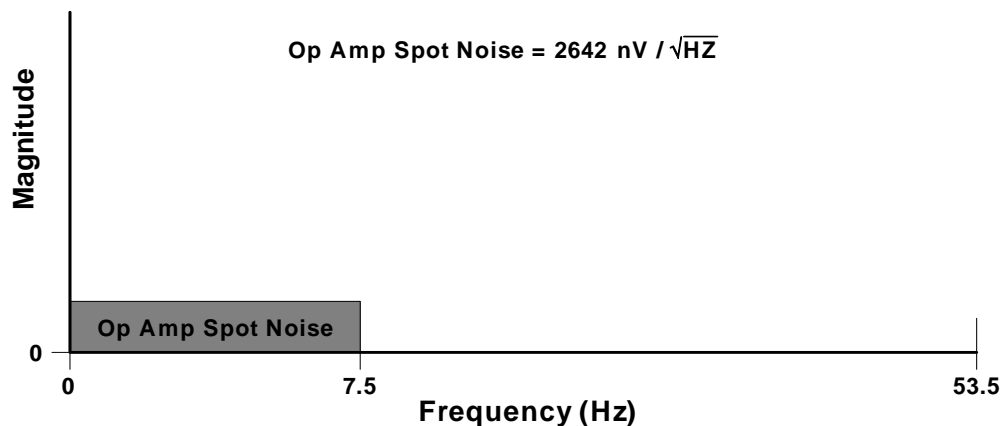


Figure 2.

This noise is that of the front end components only and does not include the noise of the ADC. The noise from the amplifier will be reduced by the RC filter corner at 4.73 Hz at a rate of about 6 dB / octave. The noise bandwidth of a single-pole filter is 1.57 times the -3 dB corner frequency, so the effective noise bandwidth for the amplifier is 7.43 Hz. A frequency of 7.5 Hz will be used for the bandwidth of the input noise and in the derivation that follows.

It is difficult to estimate spot noise (per $\sqrt{\text{Hz}}$ noise) characteristics of a delta-sigma ADC because to do so requires that the user understand the particular noise behavior of the converter for the particular configuration in which the converter is used. The spot noise can change whenever the sample rate or master clock rate is changed. And it may change if the magnitude of the voltage reference is changed. Sometimes, A/D converter vendors will supply noise plots but they may not be at the operating conditions selected by the user. It is beneficial to actually capture data and analyze the spectrum under the intended operating conditions. Figure 3 illustrates how the spot noise characteristics of two different ADCs can be quite different. The left portion of the figure illustrates the noise spectrum of a specific delta-sigma ADC along with the magnitude characteristic of its digital filter (a Sinc³ filter). As the frequency increases, the filter attenuation increases, and therefore, the noise decreases across the spectrum as the frequency approaches one half the converter sample rate as shown in the Figure 3.

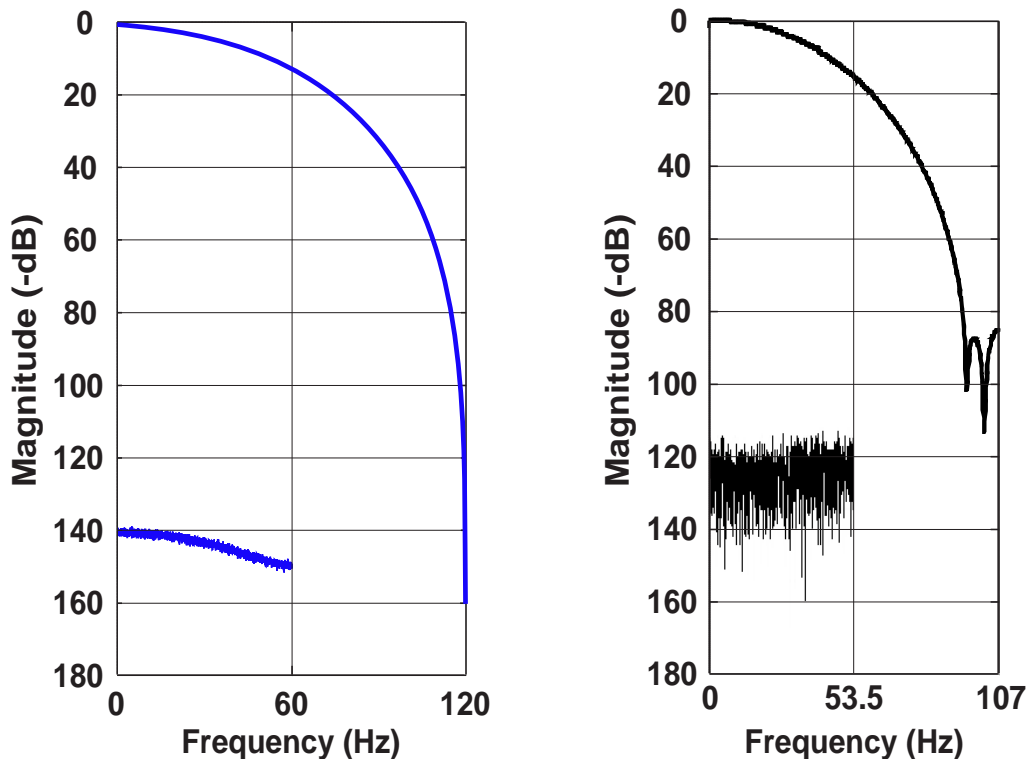


Figure 3.

In this case, the effective noise bandwidth of the digital filter would be that of the Sinc^3 filter. This is 0.275 times the sample rate. In the figure above, with a sample rate of 120 Sps, the effective noise bandwidth would be $(0.275)(120) = 33$ Hz.

The right half of Figure 3 is the noise characteristic of the CS5513 operating at 107 Sps. The noise in the CS5513 converter behaves differently than that of the ADC with the Sinc^3 filter. The CS5513 is stated to exhibit 12 microvolts rms noise in its output codes with a VREF voltage of 5 V. The CS5513 runs on an internal oscillator and its conversion rate is about 107 Sps. As shown in the spectral plot, the noise is not attenuated across the frequency spectrum. This is due to the particular design of the CS5512/CS5513 device in which some noise is aliased back into the pass-band. Because of this behavior, the noise is nearly flat across the frequency band from 0 to 53.5 Hz even though the filter has significant attenuation with increasing frequency as shown in the right portion of Figure 3.

Therefore, based upon the spectral plot for the noise which indicates that the noise is flat across frequency in the CS5513 ADC, an estimate of the noise per $\sqrt{\text{Hz}}$ would be $12 \mu\text{V} / \sqrt{(53.5)} = 1640 \text{ nV } \sqrt{\text{Hz}}$.

The noise contributed by the ADC is distributed across the spectrum up to one-half the converter output word rate. The sample rate of the CS5513 is nominally 107 Sps. This is illustrated in the following figure:

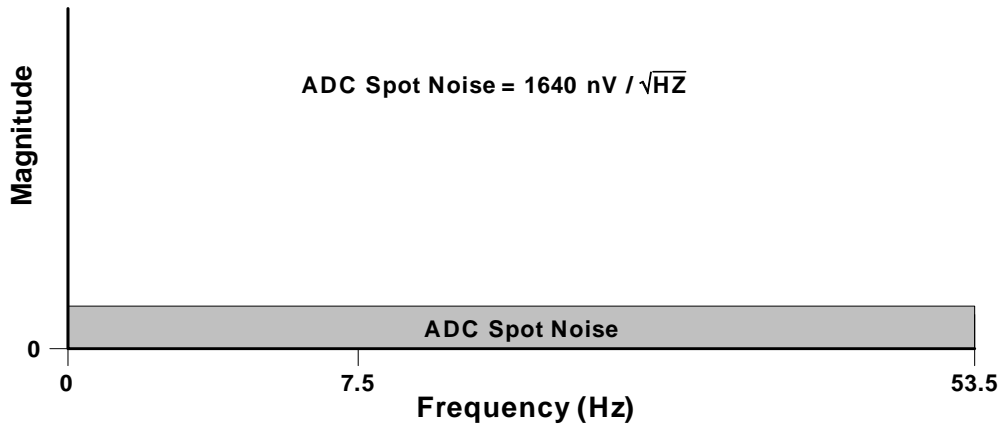


Figure 4.

As shown earlier, the op amp noise (after being amplified) is $2642 \text{ nV} / \sqrt{\text{Hz}}$, and the estimate for the ADC spot noise is $1640 / \sqrt{\text{Hz}}$. These summed together would be $(2642^2 + 1640^2) = 3110 \text{ nV} / \sqrt{\text{Hz}}$, but this is only valid for frequencies below the noise bandwidth of the analog low-pass filter. Above the noise bandwidth of the filter, only the spot noise of the ADC will be present.

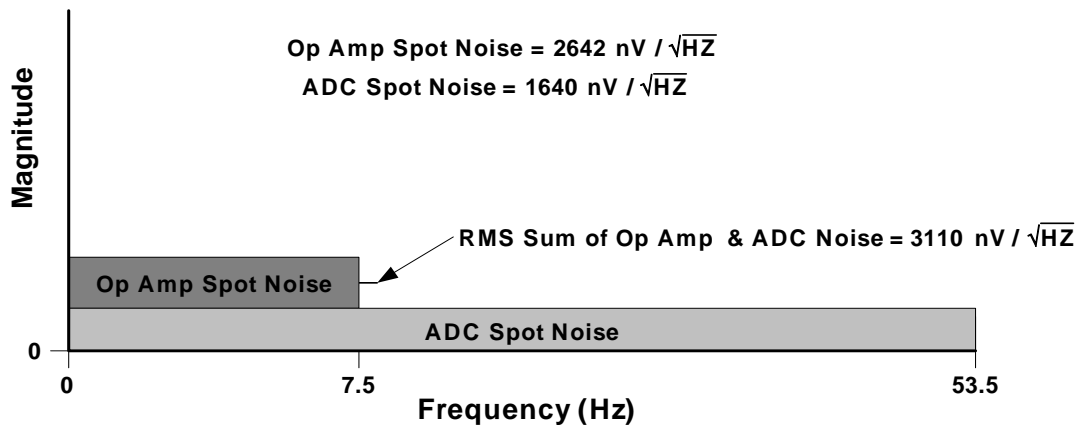


Figure 5.

The amplifier noise and the ADC noise below 7.5 Hz will add in rms fashion to produce $(2642^2 + 1640^2) = 3110 \text{ nV} / \sqrt{\text{Hz}}$. Across 7.5 Hz the total integrated noise will be $\sqrt{7.5}$ times $3110 \text{ nV} / \sqrt{\text{Hz}} = 8.52 \text{ } \mu\text{Vrms}$. The total noise from the ADC from 7.5 Hz to 53.5 Hz will be $\sqrt{(53.5 - 7.5)}$ times $1640 \text{ nV} / \sqrt{\text{Hz}} = 11.1 \text{ } \mu\text{V rms}$. Adding these two noise numbers in rms fashion will result in an estimate for the total noise exhibited by the ADC. This will be $(8.52^2 + 11.1^2) = 14 \text{ } \mu\text{V rms}$. The peak-to-peak noise would be the rms value, $14 \text{ } \mu\text{V}$, multiplied by 6.6 (± 3.3 standard deviations) or $92.4 \text{ } \mu\text{Vpeak to peak}$.

Recall that the 5 mV signal from the load cell became 2.04 volts into the ADC. Using the noise estimate one can estimate the noise-free counts from the converter as $2.04 \text{ V} / 92.4 \text{ } \mu\text{V} = 22,078$ noise-free counts out of the ADC. This is the performance on the output words of the CS5513 with no post filtering performed by the microcontroller.

This circuit with the CS3001 and the CS5513 was constructed and tested in the lab. With the input held stable, (some comments on testing will be stated later) 256 conversion words from the CS5513 were collected and the standard

deviation was calculated with a result equal to 1.8 codes. The amount of voltage represented by one code of the converter would be the full scale span of the converter (8 Vpp) divided by 2^{20} codes, or $8 / 1048576 = 7.629 \mu\text{V}$ per code. Note that one standard deviation of a Gaussian noise distribution is equivalent to the rms noise of the distribution. Therefore, with the computed standard deviation of the 256 samples equal to 1.8 codes, the rms noise of the distribution would be 1.8 times $7.623 \mu\text{V} = 13.7 \mu\text{V}$. This agrees with the calculated estimate of $14 \mu\text{V}_{\text{rms}}$.

The noise level in the output codes of the converter can be improved by using the microcontroller to perform averaging. If 20 samples at 107 Sps are averaged together, the averaging produces a sinc filter with an output rate of $107 / 20 = 5.35$ Sps. The noise bandwidth of the Sinc¹ filter would have a bandwidth of one half the output rate, or 2.67 Hz. The noise floor across this frequency was $3104 \text{ nV} / \sqrt{\text{Hz}}$, therefore the noise in this bandwidth would be about $\sqrt{2.67}$ times $3110 \text{ nV} / \sqrt{\text{Hz}} = 5.07 \mu\text{V}_{\text{rms}}$. Peak-to-peak (± 3.3 standard deviations) noise would be 30.4 microvolts. This would yield about $2.04 / 30.4 \mu\text{V} = 67,035$ noise-free counts on the 5 mV signal from the load cell.

Some comments about testing the circuit are appropriate. The circuit is amplifying very small signals. If the averaged result above is to achieve 67,035 noise-free counts, this would indicate that one noise-free code, referred to Input, is equivalent to $5 \text{ mV} / 67,035$ codes, or 75.5 nV per noise-free count. This is at a level that air currents in the room can create changes in the parasitic thermocouple connections in the circuit. Therefore, the circuit board should be covered up with a towel or put into a box and allowed to stabilize for a time before measurements are taken.

The load cell itself can be the source of unexpected spectral content in the signal. This can occur if the load cell experiences vibration. Once while performing tests with a load cell, the level of noise did not match what was expected. The cause of the discrepancy was traced to the fact that the load cell was vibrating continuously. The system was being tested on the fourth floor of an office building that had an underground parking garage. Due to automobiles moving around in the garage, the building was always subject to minute vibrations that were being sensed by the load cell. The testing had to be moved to a measurement environment on the ground floor in a different building (without an underground parking garage) to achieve the level of performance that was expected. Another recommendation to help eliminate spurious output from the load cell itself while taking noise performance measurements is to remove the load cell from its normal suspension system and to lay it on a padded surface in such a way that it is orthogonal to the direction of the normal applied force.

When collecting output data from the ADC it is always beneficial if one can actually see the shape of the distribution of the output codes. A method used to do this is described in *Appendix A. Using Excel® to Produce a Noise Histogram Plot*.

The CS3001 + CS5513 circuit uses only one op amp with the ADC. It is, therefore, a lower-cost solution, but this single-amplifier circuit has some disadvantages. First, this circuit is recommended only when the load cell is in very close proximity to the op amp. If the load cell is some distance from the op amp, this introduces the possibility of the circuit picking up interference in the wiring length from the load cell directly into the sensitive op amp inputs. Second, the temperature coefficient of the two resistors that set the gain of the circuit (the load cell resistors in parallel as the input R, and the feedback resistor around the op amp) can have different temperature coefficients. This may result in gain drift with temperature changes.

3. CS3001 AND CS5512 COMBINATION CIRCUIT WITH BRIDGE OFFSET

The second circuit is similar to the first. It uses a single CS3001 amplifier with a load cell to drive the CS5512 ADC. The CS5512 device runs from an external continuous clock which is derived from the microcontroller to the SCLK pin of the CS5512.

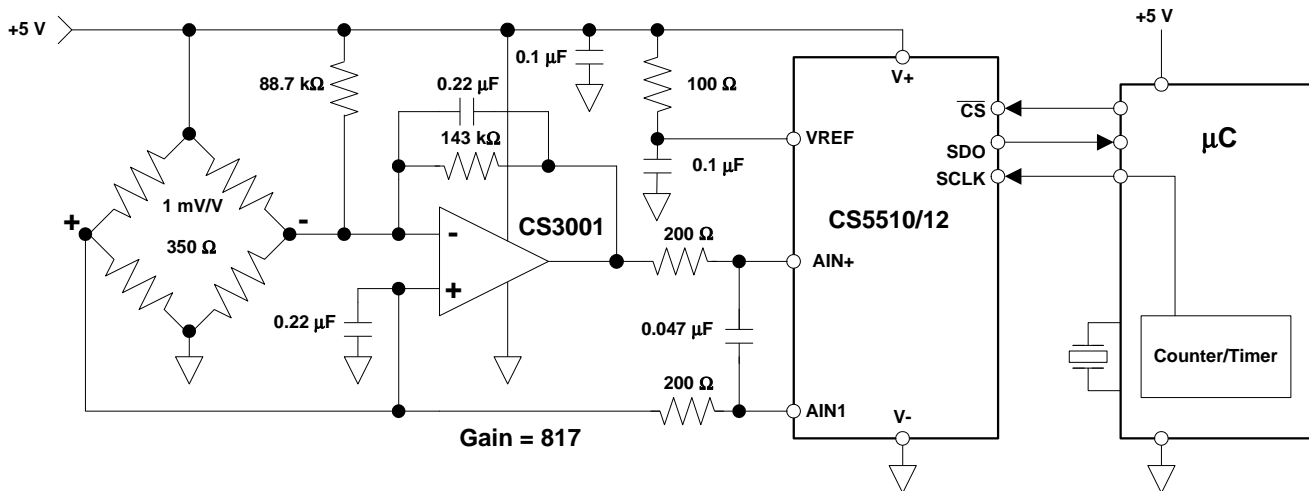


Figure 6.

The circuit shows the CS3001 set with a gain of 817X (the gain is $143\text{ k} / 175\text{ ohm}$; the 175 is set by the parallel combination of the two 350 ohm resistors inside the bridge). Note that few op amps can support a gain of 817x (58 dB) and guarantee 16-bit or better linearity; the CS3001 will exhibit a 20-bit linearity. In this circuit the 88.7 k resistor is added to offset the bridge to allow the input of the ADC to be negative with no weight on the load cell. This allows more of the input span of the A/D converter to be used. The input of the ADC is $\pm 4\text{ V}$, fully differential. Adding offset allows use of the negative range of the ADC. This provides more codes out of the converter for the bridge signal.

The bridge has a sensitivity of $1\text{ mV} / \text{V}$ so it outputs 5 mV at full scale. The noise of the amplifier is $6\text{ nV} / \sqrt{\text{Hz}}$.

The CS5512 can be driven from any clock rate from 10 kHz to 200 kHz. There are 612 clock cycles per conversion so this means the CS5512 could output conversions at rates from 16.3 Sps to 326.7 Sps by changing its clock. The noise in the converter is dominated by quantization noise and will be spread from DC to one half the output word rate. This was illustrated with the plot of the CS5513 noise in Figure 3. The CS5512 and CS5513 use the same modulator-filter design with the only difference being the clock source used to drive the chip. This means that with the CS5512, the converter can achieve a lower spot noise if the output word rate is maximized. Running the converter with a 200 kHz clock yields an output word rate of 326.7 Sps or an $F_s / 2$ bandwidth of $326.7 / 2 = 163.3\text{ Hz}$. Under this condition the spot noise (with $V_{REF} = 5\text{ V}$) would be $12\text{ }\mu\text{V rms}$ divided by the square root of 163.3 or about $939\text{ nV} / \sqrt{\text{Hz}}$. If this value is divided by 817 and referred to the input of the CS3001 amplifier the result is $1.15\text{ nV} / \sqrt{\text{Hz}}$. This is significantly below the spot noise of the op amp. Therefore, the op amp will be the dominant source of the input-referred noise.

If the clock for the CS5512 was reduced to 32.768 KHz then the spot noise of the ADC would be about $2320\text{ nV} / \sqrt{\text{Hz}}$. Referred to the input of the amplifier, this would become $2.84\text{ nV} / \sqrt{\text{Hz}}$. This would increase the input-referred noise of the system below the analog filter noise bandwidth to about $7.0\text{ nV} / \sqrt{\text{Hz}}$.

To achieve maximum signal-to-noise performance, the bandwidth of the system should be limited. The $0.22\text{ }\mu\text{F}$ capacitor across the $143\text{ k}\Omega$ resistor will limit the amplifier bandwidth to a single pole at 5 Hz. Additional filtering can be achieved by averaging the output codes of the converter. If the converter outputs words at 326.7 Sps and 32 conversion words are averaged, this will result in an effective word rate of about 10 Sps and a noise bandwidth of about 5 Hz. The signal will be 5 mV and the noise will be $7\text{ nV} / \sqrt{\text{Hz}}$ times the square root of 5, or

$7 \times \sqrt{5} = 15.7$ nVrms. The peak-to-peak noise would be 6.6 (± 3.3 standard deviations) times 15.7 nV or 103.6 nVpp. Therefore, the resulting noise-free counts would be $5 \text{ mV} / 103.6 \text{ nV} = 48,253$.

If lower-power operation is desired, the CS3011 operational amplifier could be substituted. Due to its lower operating current, the CS3011 amplifier has about 2x the noise of the CS3001. This would result in a reduction of the noise-free counts by a factor of two.

In addition to the comments about the single opamp configuration made earlier, this circuit may have an offset drift with temperature as the 88.7 k resistor temperature coefficient can be different from the load cell bridge resistors' temperature coefficients.

4. CS3002 AND CS5512 COMBINATION CIRCUIT WITH BRIDGE OFFSET

With two op amps the noise due to the amplifiers will increase by a factor of $\sqrt{2}$, (1.41). But this amplifier configuration has the advantage that each input has high impedance and it is much easier to add components to perform RFI filtering. This will be discussed in a later paragraph.

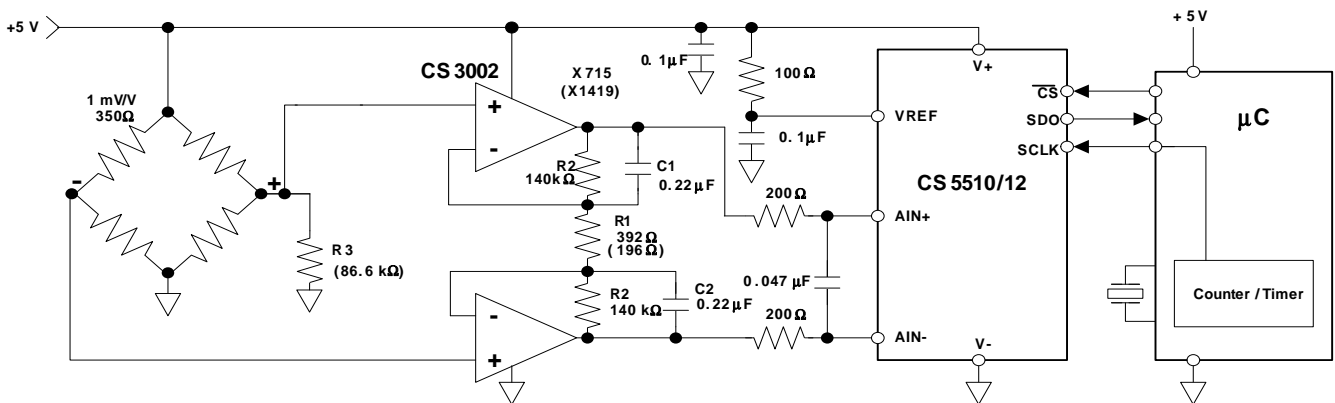


Figure 7.

In this third circuit, the CS5510/CS5512 is used in combination with the CS3002 dual op amp. Note that there is the CS3012 dual with half the power consumption but twice the noise of the CS3002 if lower power consumption is a requirement. The circuit can be configured in either of two ways, dependent upon the choice of resistors. In one configuration, the output of the bridge is amplified and input into the ADC without any offset being added. In this case, only the positive input span of the ADC is used. In the second configuration, a resistor (the 86.6 kΩ) causes the bridge to output a negative offset when no force is applied. This causes the signal into the ADC to be offset into the negative portion of the input span of the ADC. When the offset is added, the gain of the amplifier is increased to allow a much larger portion of the ADC span to be utilized.

Let's first examine the circuit without offset. In this case the gain of the amplifier is 715. The full-scale signal from the load cell under full load is 5 mV. The amplifier would then provide a full-scale signal into the ADC of 3.57 volts. This value has been chosen because the full scale of the ADC is nominally 80% of 5 V into the VREF pin but worst case can be as low as 72% (per the data sheet) so the full scale could be as low as 5 V times 0.72, or 3.6 V. In this configuration, the system would use only 3.57 volts of the nominal 8-volt span (full differential) of the converter. Note that the span could be as low as 7.2 V or as high as 8.8 V depending upon the gain error of the ADC. But if a nominal value is used, the circuit will use only 3.57 / 8 or 44.6% of the output codes of the converter. With the CS5512, this would be about 467,900 codes.

In the configuration where an offset is added to the bridge and the amplifier gain is doubled, the useful code range is doubled to about 936,000 codes.

What about noise performance? Each op amp in the CS3002 exhibits $6 \text{ nV} / \sqrt{\text{Hz}}$ up to 2 kHz bandwidth. In the differential-in-differential-out, two-amplifier configuration shown, the noise will increase by the square root of 2 to about $8.5 \text{ nV} / \sqrt{\text{Hz}}$.

In the previous circuit example it was indicated that the spot noise of the ADC would be about $939 \text{ nV} / \sqrt{\text{Hz}}$ if clocked at 200 kHz. With an amplifier gain of 715, the input-referred noise from the ADC to the input of the amplifiers would be $939 / 715 = 1.31 \text{ nV} / \sqrt{\text{Hz}}$. Adding this in rms fashion to the 8.5 nV rms noise of the amplifiers will yield about $8.6 \text{ nV} / \sqrt{\text{Hz}}$ rms.

If 32 output words were averaged, the effective output would yield results at $326 \text{ Sps} / 32 = 10.18 \text{ Sps}$ with an effective noise bandwidth of about 5 Hz.

Across 5 Hz, the integrated noise would be $\sqrt{5} \cdot 8.6 \text{ nV} / \text{Hz} = 19.5 \text{ nV rms}$. The peak-to-peak noise of the amplifier would be 6.6 times 19.2 or 126.7 nVpp. The noise-free counts would be $5 \text{ mV} / 126.7 \text{ nVpp} = 39,463$. This is across ± 3.3 standard deviations. For ± 2 standard deviations, the converter would yield 65,104 noise-free counts over 95% of the time. This would yield 16 bits noise-free on a 5 mV load cell signal.

The following figure illustrates how filter components for RFI can be easily added.

The 200 ohm resistor is chosen to minimize noise. Two capacitors are chosen, the 0.02 microfarad to provide a lower-frequency corner to the filter, and the 300 picofarad to provide much better high-frequency filtering. The 300 picofarad capacitor should be chosen from a capacitor technology that provides the highest self-resonant frequency.

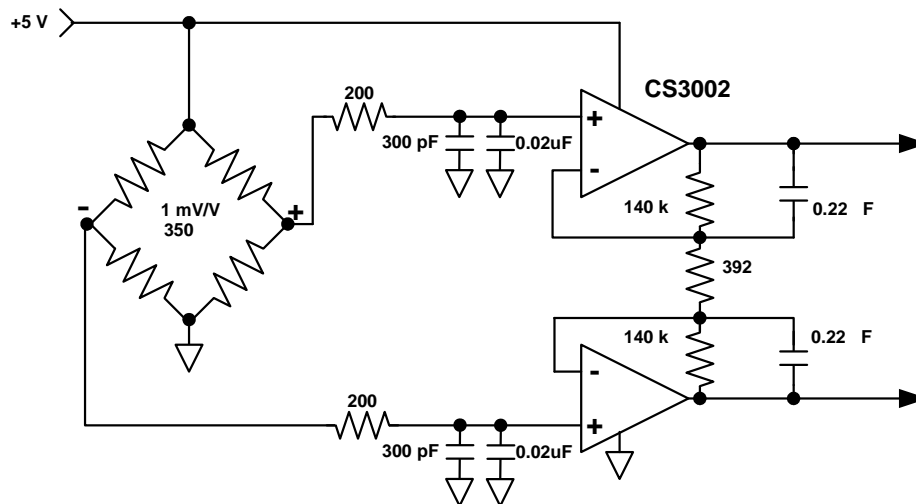


Figure 8.

This application note has illustrated several circuits that are suitable for use in battery-powered weigh scales. The application note has illustrated how noise performance can be estimated by analysis and verified by measurement.

The devices mentioned are all configured to operate with 5V supply. The devices use the following typical currents:

- CS3001 – 2.1 mA
- CS3011 – 0.9 mA
- CS3002 – 3.6 mA
- CS3012 – 1.7 mA
- CS5512 – 0.36 mA

The CS3002 and CS5512 together use about 3.96 mA typical, which results in less than 20 mW of power consumption.

APPENDIX A. USING EXCEL® TO PRODUCE A NOISE HISTOGRAM PLOT

To use Excel® spreadsheet software to produce a noise histogram plot, one must first collect data samples from the A/D output, put them into a decimal ASCII character-based format and get them into a file on a PC (personal computer). There are many ways this can be achieved, but this is left as an exercise for the reader.

The size of the data file should be at least 50 samples. However, a data file having several hundred samples is preferred. A higher number of samples will result in a higher confidence in the computed results. Note that it is common for software to collect binary multiples of samples, such as 256, 512, 1024, etc. The data can then be used for both noise histograms and for fast Fourier transform (FFT) analysis.

Once the file is on the PC, launch the Excel spreadsheet software (the following is based upon Excel 2003 with SP2) and use the *Data > Import External Data > Import Data* function to import your data file into an Excel spreadsheet. It is helpful to use either spaces or commas in your file as delimiters for each conversion word.

Our example that follows will use the 256 samples captured from the CS3001/CS5513 combo circuit mentioned at the beginning of this application note.

Once the data is entered into the spreadsheet, one can select a blank cell, then use *Insert>Function>STDEV* and select the column of data. This will compute the standard deviation (in fractions of counts) and enter the result in the selected cell.

This computation gives no indication whether the data collected actually exhibits a Gaussian or bell-shaped statistical distribution. It is beneficial to examine a plot of the collected data to ascertain whether it is in fact, a bell-shaped distribution.

In order to plot the histogram of the data collected one must first be certain that the Data Analysis Pak has been installed into the Excel software. The Data Analysis Pak comes with the Excel application but is not necessarily installed when the Excel software is installed on your PC. Therefore, look under *Tools > Data Analysis...* If *Data Analysis* is not listed, select *Add-Ins* and then highlight the box for *Analysis Pak* and click *OK*. This will install the data analysis package and should add a *Data Analysis* item under the *Tools* menu items.

Before using the Histogram function which is in the Data Analysis pak, more information is needed about the column of data that was entered into the spreadsheet from the ADC. We must know the minimum code value and the maximum code value. These can be computed by selecting a blank cell, then using *Insert>Function>MIN*. This will result in placing the minimum value of the data set in the cell which has been selected. Then select another blank cell, and use the *Insert>Function>MAX* to find the maximum value of the data set.

Once the *MIN* and the *MAX* of the data set are known, then produce a column of cells that contain a sequence of numbers from the *MIN* value to the *MAX* value incremented by one. This can be accomplished manually, or one can enter the *MIN* value into a cell, then use the *Edit > Fill > Series > Column > linear* and enter the *MAX* code value for the *Stop* value. This should result in a column of numbers starting at the *MIN* of the data set, incrementing by one up to the *MAX* of the data set.

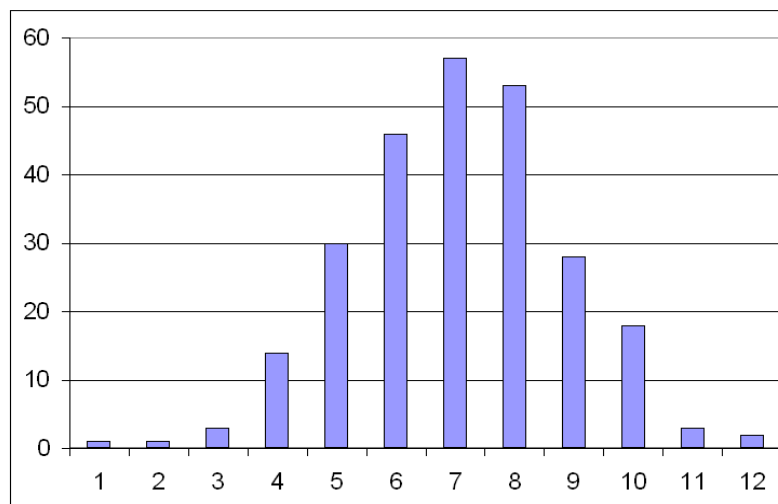
Once this is completed you should have two columns, one holding your data set of conversion output words from the ADC and a second column that increases from the *MIN* value to the *MAX* value of the data set.

Using these two columns of data one can produce a histogram frequency table. Use *Tools > Data Analysis > Histogram* Enter the spreadsheet cell range for the ADC samples in the *Input Range* selection and the *MIN* to *MAX* code range in the *Bin Range*. If the Output option *New Worksheet Ply* is selected the histogram results will appear on a new spreadsheet page.

An example which uses the 256 samples from the CS3001-CS5513 circuit yields the following result:

Chart 1		
	A	B
1	<i>Bin</i>	<i>Frequency</i>
2	3543	1
3	3544	1
4	3545	3
5	3546	14
6	3547	30
7	3548	46
8	3549	57
9	3550	53
10	3551	28
11	3552	18
12	3553	3
13	3554	2
14	More	0
15		

One can then use the *Chart Wizard* in the Excel application and the *Column Chart* option to plot the Frequency data like this:



From the plot one can easily see that the data exhibits a Normal (also called Gaussian or bell-shaped distribution) which is what should be expected if one is observing thermal noise. The histogram shows that the peak-to-peak code variation from the CS3001/CS5513 circuit is 12 codes. If this is divided into the 267387 codes used in the converter across the 2.04 volt input span, the result is 22,282 noise-free counts, which is close to what was calculated (21,935). The Excel software was used earlier to compute the standard deviation at 1.8 codes. By multiplying the standard deviation by 6.6 (± 3.3 standard deviations), the result is 11.88 codes, which agrees with the peak-to-peak range illustrated in the plot of 12 codes.

5. REVISION HISTORY

Release	Date	Changes
REV1	Oct 2008	Initial Release
REV2	Apr 2009	Minor typographical error corrected on page 5.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

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