



Integrating CobraNet™ into Audio Products

(Advice from the Experts)

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Introduction

This applications note is intended to help hardware designers integrate the CobraNet interface into an audio system design. It covers some of the finer points involved in the use of either the CS18101 device or CPB-18101-CM-2 (CM-2 module). For more detailed electrical specifications, timing diagrams, etc. please refer to the appropriate Cirrus Logic data sheet. Additional information is available from Cirrus Logic at <http://www.cirrus.com> and Cirrus Logic's Professional Audio Division at <http://www.peakaudio.com>.

Whether your design requires the ease of use and upgradability provided by the CobraNet CM-2 module or the cost-effective, on-board integration of the CS18101 and support circuitry within your product design, CobraNet technology provides a powerful, easy-to-use solution for networked audio.

The CS18101 and CM-2 module provide up to eight audio channels with input and output at 48kHz or 96kHz sampling and 32-bit resolution.

The 100Base-TX Ethernet interface is fully compliant with the IEEE802.3u standard. Remote control, monitoring, and management is accomplished through an Ethernet-based Simple Network Management Protocol (SNMP) agent. This allows the use of inexpensive category-5 cabling for new installations but the system can even be "piggy-backed" onto an existing network.

Using CobraNet Modules in Your System

Cirrus Logic, Inc. manufactures several CobraNet modules that can be integrated into your products. This is the easiest and quickest way to get CobraNet into your products. Currently, the modules that are available are the CM-1, CM-1-FW and CM-2.

The modules consist of a 3.5 x 3.5 inch PCB. One or more connectors or connection points are used to connect to a standard Ethernet network. A pair of high density connections are used to interface the module to the host system. An optional metal faceplate is used to facilitate mounting the module to the chassis. Details for these modules can be found in the appropriate module's data sheet.

Note: This applications note is intended to supplement the data sheets. It is not intended to replace or supersede the data sheets. Also, these are guidelines only and do not apply to all situations.

Power

The CM-1 and CM-1-FW use both +3.3v and +5.0v power supplies. The CM-2 requires a single +3.3v supply. We do not anticipate any future CobraNet modules will require the +5v power supply. If you do not believe your design will ever use the CM-1 or CM-1-FW, leaving the +5v pins un-powered is acceptable. However, we recommend that if +5v power is already available within your system, it should be connected.

Maintaining Signal Quality

Maintaining signal quality is essential for proper operation, meeting FCC/CE emission requirements, and for overall reliability. Experience has shown that the vast majority of CobraNet hardware problems have come from lack of signal and power quality. This isn't because implementing and using CobraNet is difficult, but rather that many electrical engineers that design audio products are unfamiliar with high-speed digital logic (and the analog effects of high-speed digital logic). What follows is the "accumulated wisdom" from years of designing and debugging CobraNet products.

De-coupling capacitors (sometimes called AC signal return caps or bypass caps) are critical for maintaining signal and power quality. Since the CobraNet modules run at high speeds and the digital signals have very short rise/fall times, de-coupling caps cannot be ignored.

On the host PCB, connect six 0.1uF caps between +3.3v and Ground. Distribute these caps across the length of the connectors, keeping them as close to the connectors as possible. Also connect a single 0.1uF cap between +5v and Ground at the +5v pins on the connector. Even if you are using only the CM-2, which does not require +5v, the cap on +5v must still be present. And even if your host board does not have a +5v power rail available, connect the cap between the +5v pins and Ground (while leaving the +5v pins un-powered).

These caps reduce the AC signal return path, thus reducing EMI and improving signal quality. The pinout of the module host connector is optimized for signal quality and assumes that these caps will be used on the host PCB.

Signals to and from the module should be kept as short as possible. High-speed traces on the host board longer than about 4 inches should be avoided or use buffers. Keep in mind that "high speed" in this case refers to signals with short rise and fall times, not just the frequency of the signal.

Loading and Termination

Signals to and from the module should have only a single load. This is true for outputs as well as inputs. In the case of an output from the module having multiple loads, a buffer should be used. If the signal is an input to the module then there should be no additional loads on that signal on the host PCB. Obviously there are situations where this rule can be relaxed, but more often than not this is the case.

Pay close attention to signal termination on the *MCLK_OUT* (*FS512_OUT*), *FS1*, and *SSI_CLK* signals. If these signals are used as outputs from the module to your host PCB then the board must include some sort of R-C termination at the end of the trace. On the other hand, if these signals are inputs to the module from the host PCB then we recommend using series termination at the driver.

The CM-2 has 25Ω source-termination resistors on the *SSI_CLK* and *FS1* signals to improve signal quality. On some systems, this may conflict with some end termination schemes.

Special Signals

The CM-1 (and CM-1-FW) pin *RSVD0* is used as *HADDR3* on the CM-2 and there is a pull-down resistor on it. We recommend that new designs connect to *HADDR3* even if the design will never use the CM-2, since future CobraNet Modules will likely use *HADDR3*.

If pull-up or pull-down resistors are placed on the *SSI_DOUT* signals (in the event that the CobraNet module is not installed), these resistors should be very weak (greater than 50kΩ). There are already pull-up and pull-down resistors on the CobraNet module so any additional resistors should be sufficiently weak to not interfere.

Unlike the CM-1, the *HEN#* signal is used on the CM-2. CM-1 documentation has recommended that the *HEN#* be tied low on the CM-1. This recommendation is compatible with the CM-2.

Integrating CobraNet Circuitry into PCBs

There are several advantages to integrating the CobraNet circuitry into your own PCB rather than using one of the CobraNet modules. Signal quality, higher integration, and lower cost are just some of them.

Integrating the CM-1 Circuit

The CM-1 is a challenging circuit to integrate. We do not recommend integrating this circuit unless it is absolutely necessary. If design requirements necessitate integration, it should be done with a great deal of care. It is not impossible to integrate, just very difficult given the level of technology used. If integration of the CM-1 circuit is necessary, contacting Cirrus Logic, Inc. support is highly recommended.

Integrating the CM-2 Circuit (using the CS18101)

Unlike the CM-1, the CM-2 (and thus, the CS18101) is very integration friendly. The circuit is much simpler and has fewer high-speed signals. In most cases it makes more sense to integrate the CM-2 than to use the module.

What follows are some design notes on integrating the CM-2 circuit into a PCB.

The CM-2 has a voltage regulator that converts +3.3 volts to +1.8 volts. The regulator on the CM-2 is a high-efficiency switching regulator. This regulator is more expensive than a basic low-dropout linear regulator, but dissipates less power (0.1 watts vs. 0.75 watts). In a PCB design, a linear regulator can easily be used if cost is more important than power consumption. Also, this voltage regulator can be omitted if a +1.8v power rail already exists in the design.

The CM-2 contains a second Ethernet controller and connector. If these are not required they can simply be removed from the design. In this case, all devices and circuits referenced on the "*Secondary Ethernet*" schematic page can be omitted.

It is not recommended to replace the 10uF ceramic capacitors with tantalum or aluminum electrolytic. The ceramic caps have superior performance and life span, as well as smaller size than either tantalum or aluminum electrolytic capacitors. It's also important to make sure that any voltage regulator used will work properly with these ceramic caps.

If power will not be supplied via the Ethernet cable then consider using a different Ethernet connector that includes the termination resistors and caps in the connector. This should lower EMI, reduce parts count, and reduce PCB size.

The CM-2 is designed with termination on only a few of the signals. This is possible because the PCB layout keeps the signal traces short. If the design requires longer traces, selectively terminating some of the signals may be required.

The CM-2 uses capacitor arrays rather than individual capacitors. This works well when the caps are placed on the bottom of the PCB, below the ICs. When the caps are placed

on the same side as the ICs, individual caps work better since it allows for a more even distribution around the ICs.

The CM-2 module was designed using a 6-layer PCB and 6-mil traces. This is due to the amount of circuitry packed into the small PCB. If the PCB were larger, or the second Ethernet connector removed, a 4-layer PCB would have been adequate. However, we do not recommend using a 2-layer PCB.

Thermal

While the CobraNet modules and the CS18101 are relatively low-power devices, heat dissipation can not be ignored. If the system will be in a sealed case with no ventilation and/or your host board is dissipating some heat then it is necessary to plan for system cooling.

Thermal analysis of a complete system is complex and difficult. Like EMI, the theory behind it is well understood and documented but the practical application of it is more of an art than a science. This applications note shows the thermal analysis of the CM-1 and CM-2 and what its practical effects are.

The Theory

There are many factors that effect the thermal performance of a circuit. The major ones are power consumption, ambient temperature, and airflow/convection. Lesser factors include humidity, air turbulence, PCB construction, and thermal conductivity of all parts. But none of these describes how a circuit might fail due to high temperatures.

As a semiconductor heats up it slows down. If it slows down too much then it will start to exceed the timing margins and the logic will fail. This failure is dependant on the temperature of the semiconductor die, also called the "junction temperature". The junction temperature is dependant on the power being dissipated in the die and how fast that heat can be removed from the die through the chip package.

The basic formulas governing this are:

$$\theta_{ja} = (T_j - T_a) / P_d$$

$$\theta_{jc} = (T_j - T_c) / P_d$$

Where:

T_j is the junction temperature, in °C.

T_a is the ambient air temperature, in °C.

P_d is the power being dissipated by the chip, in watts.

θ_{ja} is the thermal coefficient between the junction and ambient temperature, in °C/Watt.

θ_{jc} is the thermal coefficient between the junction and case temperature, in °C/Watt.

Normally, T_{ja} , T_{jc} , and P_d are provided in the data sheets for the chip in question. So using the above formulas we can calculate the junction temperature of each chip and determine if it is above the maximum value stated in the data sheet. Easy, right? Well...

The Practice

Theory is good, but it falls well short in practice. For starters, the results are only as good as the data and the data is often missing or questionable. T_{ja} , T_{jc} and $T_j(\text{max})$ are often missing from the data sheets altogether. And when they are listed T_{ja} and T_{jc} often have a wide error margin. To make matters worse, P_d is sometimes no better than a guess based on some ad-hoc test dreamed up by the semiconductor maker.

There are many different numbers that can be used for T_{ja} . Good data sheets list several types of thermal coefficients for different airflow rates. Mediocre data sheets will list only one T_{ja} , and it will probably be unqualified as to what conditions for which that coefficient is valid.

Then there are the factors that are not accounted for. For example, the PCB itself will act as a heat sink of sorts. This is especially true of multi-layer PCB's with many power and ground planes and BGAs that have good thermal coupling between the die and the PCB. Humidity will greatly effect the thermal conductivity of the air, as anyone living in Phoenix, Arizona can attest. And the turbulence of the air flow can play a huge role in cooling off a chip.

So what is an engineer to do? Going through the numbers will put you into the right ballpark, but testing is required to be confident that it will work.

CM-1

The CM-1 is a good example of why thermal theory and practice are not the same thing.

Of the major components on the CM-1, the SRAM, Ethernet Controller, and Ethernet are all rated at a maximum of 70°C ambient. Their data sheets list no more information on the maximum junction temperature or thermal coefficients. Further, the ambient temperature specification makes no mention of the ambient conditions (air flow, humidity, etc.). For these parts we have to assume that 70°C max. ambient under any condition is valid.

On the other hand, the FPGA and DSP have some data, which we'll go over here.

According to the Motorola 56303 data sheets:

$$T_j(\text{max}) = 100^\circ\text{C}.$$

$$P_d(\text{typ}) = 0.5 \text{ watts}.$$

$$T_{ja} = 58^\circ\text{C/Watt}.$$

Therefore:

$$T_a(\text{max}) = T_j(\text{max}) - (T_{ja}(\text{max}) * P_d(\text{typ})) = 100 - (58 * 0.5) = 71^\circ\text{C}$$

From this we can conclude that 71°C is the maximum ambient temperature allowed with this DSP. But keep in mind that P_d is a rough guess and T_{ja} is unqualified as to air flow and humidity.

Similarly, according to the Xilinx documentation:

$$T_j(\text{max}) = 100^\circ\text{C}.$$

$$P_d(\text{typ}) = 1.0 \text{ watt}.$$

$$T_{ja}(\text{max}) = 33.6^\circ\text{C/Watt.}$$

$$T_{ja}(\text{typ}) = 33.6^\circ\text{C/Watt.}$$

Therefore:

$$T_a(\text{max}) = T_j(\text{max}) - (T_{ja}(\text{max}) * P_d(\text{typ})) = 100 - (33.6 * 1.0) = 66.4^\circ\text{C}$$

According to the math we are not above the 70°C spec on the CM-1. That is because the math above does not take into account the heat-sink effect of the PCB. Under the FPGA are four copper planes and 49 vias that transport the heat to those copper planes. There are four more signal layers that also aid in heat conduction away from the FPGA.

There is not enough data to allow us to calculate the cooling effects of the PCB. And getting this data would be extraordinarily difficult. In this case we are assuming that the PCB gives us that extra 3.6°C of cooling that we need. While such an assumption might seem cavalier, 3.6° is within the margin of error for the other numbers used in our calculations. This is why we can only use the numbers for a ballpark estimate and need to do testing for final acceptance.

Another issue is the $T_j(\text{max})$ spec of the FPGA. Above it was listed as 100°C, but the data sheets list it as 85°C. The truth is that the absolute maximum is 125°C, but the timing specifications are only guaranteed to 85°C. Above that the FPGA slows down at a rate of 0.35% for every degree above 85°C. We have designed the FPGA to run at 100 MHz, 85°C. But, except for some custom firmware, we are running the FPGA at 95 MHz. So if we account for this thermal de-rating then we can calculate that a $T_j(\text{max})$ spec of 100°C is correct.

If we take the lowest common denominator of all the chips on the CM-1 we find that our ambient temperature spec is 70°C. In the case of the FPGA we know that we're talking about still air, but we really don't know what "ambient air" is with regard to the other chips on the CM-1. This is where testing can really clear things up. Testing with a still air ambient temp at 70°C and above can help to verify proper operation.

In our labs we have done elevated testing of the CM-1 to well beyond 70°C ambient without failures. Unfortunately, this doesn't mean that the CM-1 will work in your system at temperatures beyond 70°C. As has been pointed out before, there are lots of variables and only system testing can prove or disprove that it works. So we encourage all users to do their own testing.

CM-2

Since the CM-2, and the main chip on it (the CS18101) have not been completely characterized it is difficult to do any sort of analysis on it at this point. But we do have some preliminary information:

The designers of the CS18101 have said that the part will be able to operate with an ambient temp of 70°C. Based on the information available, this seems like an achievable goal.

The Ethernet Mac/Phy, the Davicom DM9000E, is rated at 0-85°C case temperature with zero air flow. Further information is needed to calculate an ambient temperature from that case temperature. But based on the chips power consumption (0.33 watts) it seems very likely that this part will work fine with a 70°C ambient environment.

There are not many other parts on the CM-2, and all of them are low-power enough to not worry about.

How To Test

There are so many factors that were not, and could not be, considered in this thermal analysis that testing should be considered.

The first question to answer is, "Do I need to test at all?"

It seems that if the ambient temperature is below approximately 55°C then you probably do not need to extensive tests. (The ambient temperature should be measured about 0.25 inches above the FPGA on the CM-1 or the DSP on the CM-2.) If past experience can be a guide then it would indicate that units with fans don't need testing while units without fans do. However, using the internal ambient temperature is a better benchmark for this sort of thing.

If you have determined the necessity to test, the next question is, "How do I test?"

Measuring things like the case temperature of the individual chips is not very helpful. Usually the temperature probes are taped to the chip (which insulates it, making it hotter), and we're not really interested in the case temperature anyway since it is the junction temperature that directly reflects the failure point. And it is difficult to calculate the junction temp from the case temp unless you know exactly how much power the chip is dissipating (which we don't know exactly).

A basic, but effective, test would be to put the unit (case and all) inside an environmental test chamber. One or more temperature probes would be placed inside the unit to measure the ambient temps at various locations.

The temp inside the chamber (inside the chamber, but outside of the unit) would be raised to about 50°C (122°F) and kept there for several hours while the unit was run through some functional tests. If all goes well the temperature would be raised 5 or 10°C and the test repeated. Tests would be run at ever increasing temperatures until the unit failed.

If the temperatures recorded during the tests are acceptable then you're done! Otherwise, you need to fix things (which is beyond the scope of this document).

What if you don't have a thermal test chamber? Then it's time to improvise. A basic one can be built using a cardboard box lined with thick foam insulating sheets (available at most home improvement stores). Inside the box put an incandescent lamp, a small fan, and some sort of thermal mass (a large bench vise or a jug of water in a well sealed container works well). This sort of setup is cheap, but it works. There isn't a thermostat, but it heats up and cools down slowly so a "manual thermostat" is good enough. If buying a real test chamber for thousands of dollars is out of the question then this might be just the ticket.

Conclusion

The practical results of all this analysis is that the CM-1 and CM-2 modules should operate just fine in an environment of 70°C ambient still air, but you need to do proper testing to verify that everything works properly.

EMI

Like thermal issues, the theory of EMI is well known but the practice is something else entirely. There are so many factors that can effect EMI that dealing with EMI can be akin to black magic. In fact, the title of a good book on EMI reflects that (and we highly recommend that book):

High Speed Digital Design: A Handbook of Black Magic
Howard W. Johnson & Martin Graham
Prentice-Hall, Inc.
ISBN: 0-13-395724-1

We won't attempt to explain how to solve EMI issues, since someone already wrote that book. But we will go over some things specific to the CobraNet Modules that may help with EMI.

Follow the section "*Maintaining Signal Quality*" above. Proper signal termination, signal loading, de-coupling, etc. can all have a dramatic effect on EMI.

CobraNet Modules have zero-ohm resistors and/or caps that connect chassis ground, digital ground, and various mounting holes. Depending on the situation, it might be advantageous to remove or change these components.

The module faceplate (or the RJ-45 connectors, if you're not using the faceplate) must make good electrical contact with the chassis. It's common for paint or other "debris" to cause electrical isolation, increasing EMI. During testing, you can try to use copper tape to make and seal this connection. A bad connection here can increase radiated emissions by 6db or more!

If possible, don't use a ribbon cable to connect the module to the host system. A direct connection will work much better, both from a signal-quality point of view as well as an EMI point of view.

When doing EMI testing, try a wide range of Ethernet switches. Experience has shown that different switches can have as much as a 12db difference in common mode emissions. So try different switches until a "good one" is found.

Your choice of power supply can also effect EMI and common mode emissions. Choose a good one!

FAQ

The following are some frequently asked questions about the CM-2.

Q: Does the CM-2 make the CM-1 obsolete?

A: No! The CM-2 does not offer the number of audio channels that the CM-1 does. For this reason (and others) the CM-1 will remain in production.

Q: Can a host system be made to use either the CM-1 or the CM-2?

A: Yes. The electrical interfaces are almost identical, and with a little software design effort either can be made to work. This way a designer can develop a "low-channel-count" version of a design that uses the CM-2 and a "high-channel-count" version that uses the CM-1.

Q: What benefits are there to using the CM-2 module rather than embedding the CM-2 circuit on my own board?

A: If the CM-2 module is used then it can be an optional add-on to your "box". It also allows you to use the CM-1 or possibly future CobraNet Modules without major redesign.

Additionally, you can customize the circuit to better match your target price point and feature set. For example, by removing the redundant Ethernet connector or replacing the switching DC/DC converter with a cheaper linear regulator, the cost and size of your system is reduced.

Q: If I embed the CM-2 circuit into my PCB design, what board qualities should I expect to need?

A: The CM-2 module is a 6-layer board with 6-mil traces and spaces. This is what we recommend people use if embedding the CM-2 circuit into their design. The CM-2 module also has some small components on the back side of the PCB, which we also recommend. If the redundant Ethernet connector will be omitted, it might be possible to put all components on the top side of the PCB and use a 4-layer board. However, we have not tried this ourselves.

Q: Why does the CM-2 (and the CM-1) use a 24.576MHz master audio clock rather than a more typical 12.288MHz clock?

A: 12.288MHz clocks are not as well suited for some phase-locked loops (PLLs). Specifically, the PLLs in Xilinx FPGAs cannot operate with a 12.288MHz clock. Also, other PLLs which may work do operate better with the higher clock.

Q: Should I use 3.3v or 5v logic when interfacing to the CM-2 (or CM-1)?

A: The CM-1 and CM-2 interface with 3.3v logic levels, but all the inputs are 5v tolerant. That being said, every effort should be made to phase out 5v circuits. Today the only major reason to use 5 volts is when interfacing to some audio converters, but all other logic is available at 3.3 volts. By using 3.3 volts you lower power consumption, lower EMI, and can use higher-speed logic. Additionally, future CobraNet modules might not be +5v tolerant on the inputs.

Q: Why blue PCBs?

A: Green is so overdone. We have gotten tired of green. Red is certainly different but a little too racy for our conservative engineers. Blue is elegant, soothing, and quite attractive!

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com

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