WAN-0129

Decoupling and Layout Methodology for Wolfson DACs, ADCs and CODECs

INTRODUCTION

This application note looks at the general decoupling and layout practice required for Wolfson converters to achieve maximum performance in a typical high-speed mixed-signal circuit.

APPLICATION

Wolfson DACs, ADCs and CODECs have both digital and analogue interfaces. It is important that noise is minimised to get the maximum converter performance. In our datasheets there are a number of supply pins on each chip. They are labelled according to their internal connection, not necessarily how they should be connected externally. The datasheets show typical supply connections and decoupling arrangements and this report goes into further details.

GROUNDING

First consider the grounding of the IC. Ideally the circuit board will have a single continuous ground plane, with all ground pins connected to it. The components will be located so that high-speed digital devices are kept away from analogue devices, so that noise currents do not stray where they are not wanted.

In some cases a cut between analogue and digital planes is required, because the component positions cannot be optimised. In this case the analogue and digital grounds must be connected under the converter with a wide copper track. Just using a zero-ohm link may not provide a good enough connection in some circumstances. Ensure any tracks going from the board's analogue section to the digital section (e.g. data lines and clocks) are tracked over the ground connection, not the cut, to minimise loop area for the return currents. Wolfson converters are designed with a pin-out which ensures tracks need only go over the appropriate ground plane. If you have other high-speed currents (including ESD currents) flowing between analogue and digital grounds, make sure this is not the only connection between them, or you will make the converter performance worse.

DIGITAL SUPPLY

Digital supply pins can be connected to the main digital supply rail if the noise levels are not too high. If there is no nearby digital supply, or it is too noisy, then one can be made from the analogue supply using an LC filter like below: this will make sure the noise does not go back to the analogue supply.

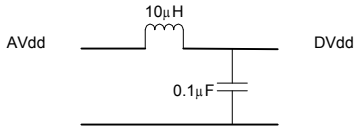

Figure 1 Converter Digital Supply from Analogue Supply

We name the digital pins like this: DVDD, DCVDD. Be sure to place a 0.1µF multi-layer ceramic capacitor close to each of these pins (within 3mm) to decouple it properly to DGND. If there is no large-value capacitor within 50mm, then also add one 10µF low-ESR capacitor per rail. This can be multi-layer ceramic, low-ESR tantalum or low-ESR organic semiconductor electrolytic type. Check the datasheet shows the part has less than 200mΩ ESR for best performance.

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ANALOGUE SUPPLY

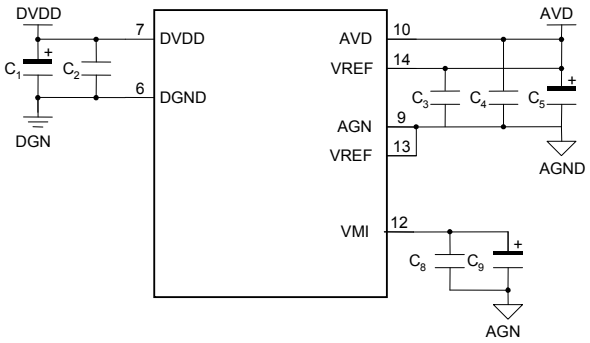
Analogue supply pins must be connected to a low-noise analogue supply rail, which ideally comes from a low-noise linear regulator. We name these pins like this: AVDD, HPVDD, SPKVDD. Be sure to place a 0.1µF multi-layer ceramic capacitor close to each of these pins (within 3mm) to decouple it properly to AGND. If there is no large-value capacitor within 50mm, then also add one 10µF low-ESR capacitor per rail. This can be multi-layer ceramic, low-ESR tantalum or low-ESR organic semiconductor electrolytic type. Check the datasheet shows the part has less than 200mΩ ESR for best performance.

On some of our devices there are internal supplies or references which require external decoupling. We names these pins like: VMID, VREF, VREFOUT, CAP2. The pins connect just to a capacitor, not to an external supply. Be sure to place a 0.1µF multi-layer ceramic capacitor close to each of these pins (within 3mm) to decouple it properly to AGND. Also add one 10µF low-ESR capacitor per pin. This can be multi-layer ceramic, low-ESR tantalum or low-ESR organic semiconductor electrolytic type. Check the datasheet shows the part has less than 200mΩ ESR for best performance.

SUPPLY LAYOUT

Ideally the supply connections will be made with planes on a multi-layer circuit board. If these planes are on adjacent layers, the parasitic capacitance of these layers will further improve high-frequency decoupling. Where this is not possible, use tracks much wider than the current rating requires.

SOLUTION



Notes:
1. AGND and DGND should be connected as close to the IC as possible.
2. $_2$, C_3, C_4 and C_8 should be 0.1µF multi-layer ceramics, positioned as close to the IC as
3. Capacitor types for C_1, C_5, C_9 should be carefully chosen. 10µF capacitors with low ESR are recommended for optimum performance.

Figure 2 Decoupling Example

CONCLUSION

With careful consideration of layout and provision of low-noise supplies, the performance specified in our datasheets should be achieved.

TECHNICAL SUPPORT

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