WAN_0204

WM9081 Control Write Sequencer Default Sequences

INTRODUCTION

Software development time and demands on the host processor can be minimised through the use the WM9081 integrated Control Write Sequencer. The Control Write Sequencer forms part of the control interface logic and can be used to enable and disable a number of signal paths (such as DAC to speaker modes) by just a single register write. The internal sequencer takes care of this by initiating a sequence of pre-programmed register writes independently within the WM9081, minimising control interface communication between the processor and WM9081.

Default sequences for controlling the Speaker and Lineout signal paths are provided (see "Detailed Sequence Descriptions" section).

When a sequence is initiated, the sequencer performs a series of pre-defined register writes. The host processor informs the sequencer of the start index of the required sequence within the sequencer's memory. At each step of the sequence, the contents of the selected register fields are read from the sequencer's memory and copied into the WM9081 control registers. This continues sequentially through the sequencer's memory until an "End of Sequence" bit is encountered; at this point, the sequencer stops and an Interrupt status flag is asserted. For cases where the timing of the write sequence is important, the sequencer is pre-programmed with time delays for specific steps within the sequence.

This document describes the default sequences which can be executed by the Control Write Sequencer. For details on using the Control Write Sequencer and initiating a sequence, please refer to the "Control Write Sequencer" section in the WM9081 datasheet.

DETAILED SEQUENCE DESCRIPTIONS

When the WM9081 is powered up, a number of default Control Write Sequences are available in non-volatile memory. The pre-programmed default settings include Start-Up and Shut-Down sequences for each of the output drivers. Note that the internal clock, CLK_SYS, must be enabled in order to run these sequences.

The following default control sequences are provided:

1. Class D Speaker Enable - This sequence powers up the speaker driver in Class D mode, and enables the DAC signal path. The soft-start VMID circuit is selected as part of this sequence. On completion, the Lineout is clamped to VMID.

2. Class D Speaker Disable - This sequence powers down the Class D speaker driver. As part of this sequence, the DAC is muted and disabled, the Lineout is discharged to AGND and the reference/bias circuits are disabled. This sequence is applicable to the Class D speaker mode.

3. Lineout Enable - This sequence powers up the lineout, and enables the DAC signal path. The lineout is discharged initially, and the soft-start VMID circuit is used to suppress pops during power-up.

4. Lineout Disable - This sequence powers down the lineout. As part of this sequence, the DAC is muted and disabled, the Lineout is discharged to AGND and the reference/bias circuits are disabled.

5. Class AB Speaker Enable - This sequence powers up the speaker driver in Class AB mode, and enables the DAC signal path. The soft-start VMID circuit is selected as part of this sequence. On completion, the Lineout is clamped to VMID.

6. Class AB Speaker Disable - This sequence powers down the Class AB speaker driver. As part of this sequence, the DAC is muted and disabled, the Lineout is discharged to AGND and the reference/bias circuits are disabled.

Specific details of each of these sequences are provided below:

1. CLASS D SPEAKER ENABLE SEQUENCE

The Class D Speaker Enable sequence is initiated by writing 8100h to Register 38 (26h). This operation starts the Control Write Sequencer at Index Address 0 (00h) and executes the sequence defined in Table 1. For typical clocking configurations with MCLK=12.288MHz, this sequence takes approximately 42ms to run.

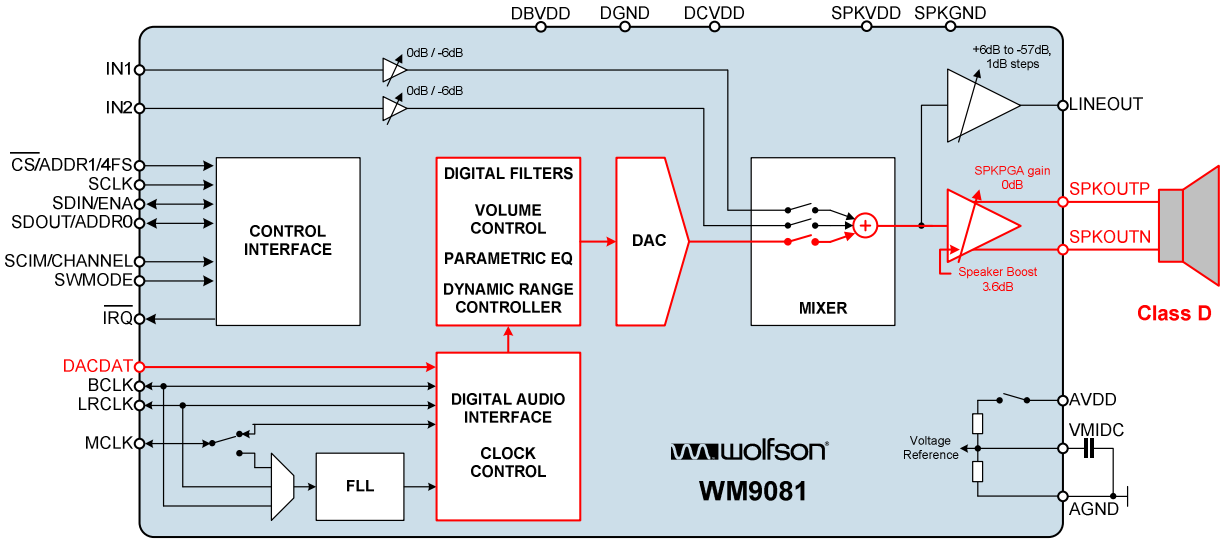

Figure 1 Signal Path: Sequence 1

Note that this sequence is optimized for pop suppression on the Speaker output. For pop suppression on the Line Output, please refer to sequence 3.

STEP	REGISTER ADDRESS	BIT	DESCRIPTION
1	R4 (04h)	3:0	VMID_RAMP = 1 VMID_FAST_ST = 1
2	R8 (08h)	2	LINEOUT_DISCH = 1
3	R11 (0Bh)	4	LINEOUT_ENA = 1
4	R8 (08h)	2	LINEOUT_DISCH = 0
5	R5 (05h)	6:0	BIAS_SRC = 0 STBY_BIAS_LVL = 1 STBY_BIAS_ENA = 0 BIAS_LVL = 10 BIAS_ENA = 1 STARTUP_BIAS_ENA = 1
6	R4 (04h)	2:1	VMID_SEL [1:0] = 01 Delay = 32ms
7	R4 (04h)	5:3	VMID_BUF_ENA = 1 VMID_RAMP = 0
8	R14 (0Eh)	1	CLK_DSP_ENA = 1
9	R11 (0Bh)	0	DAC_ENA = 1
10	R7 (07h)	4	DAC_SEL = 1
11	R11 (0Bh)	2	SPKPGA_ENA = 1
12	R3 (03h)	7	SPKPGA_MUTE = 0
13	R11 (0Bh)	1	SPK_ENA = 1 Delay = 1.5ms
14	R8 (08h)	0	LINEOUT_CLAMP = 1
15	R11 (0Bh)	4	LINEOUT_ENA = 0
16	R31 (1Fh)	9:3	DAC_MUTEMODE = 1 DAC_MUTE = 0 End of Sequence

Table 1 Sequence 1

2. CLASS D SPEAKER DISABLE SEQUENCE

The Class D Speaker Disable sequence is initiated by writing 8115h to Register 38 (26h). This single operation starts the Control Write Sequencer at Index Address 21 (15h) and executes the sequence defined in Table 2. For typical clocking configurations with MCLK=12.288MHz, this sequence takes approximately 48ms to run.

STEP	REGISTER ADDRESS	BIT	DESCRIPTION
1	R4 (04h)	3:0	VMID_RAMP = 1 VMID_SEL [1:0] = 01 VMID_FAST_ST = 1
2	R5 (05h)	1:0	BIAS_ENA = 1 STARTUP_BIAS_ENA = 1
3	R31 (1Fh)	9:3	DAC_MUTEMODE = 1 DAC_MUTE = 1 Delay = 8.5ms
4	R3 (03h)	7	SPKPGA_MUTE = 1
5	R11 (0Bh)	4:1	LINEOUT_ENA = 1 SPKPGA_ENA = 1 SPK_ENA = 0
6	R2 (02h)	7	LINEOUT_MUTE = 1
7	R8 (08h)	0	LINEOUT_CLAMP = 0
8	R4 (04h)	2:1	VMID_SEL [1:0] = 00 Delay = 32ms
9	R11 (0Bh)	4:2	LINEOUT_ENA = 0 SPKPGA_ENA = 0
10	R8 (08h)	2	LINEOUT_DISCH = 1
11	R7 (07h)	4	DAC_SEL = 0
12	R11 (0Bh)	0	DAC_ENA = 0
13	R14 (0Eh)	1	CLK_DSP_ENA = 0
14	R4 (04h)	3	VMID_RAMP = 0
15	R5 (05h)	1:0	BIAS_ENA = 0 STARTUP_BIAS_ENA = 0 End of Sequence

Table 2 Sequence 2

3. LINEOUT ENABLE SEQUENCE

The Lineout Enable sequence is initiated by writing 812Ah to Register 38 (26h). This operation starts the Control Write Sequencer at Index Address 42 (2Ah) and executes the sequence defined in Table 3. For typical clocking configurations with MCLK=12.288MHz, this sequence takes approximately 550ms to run.

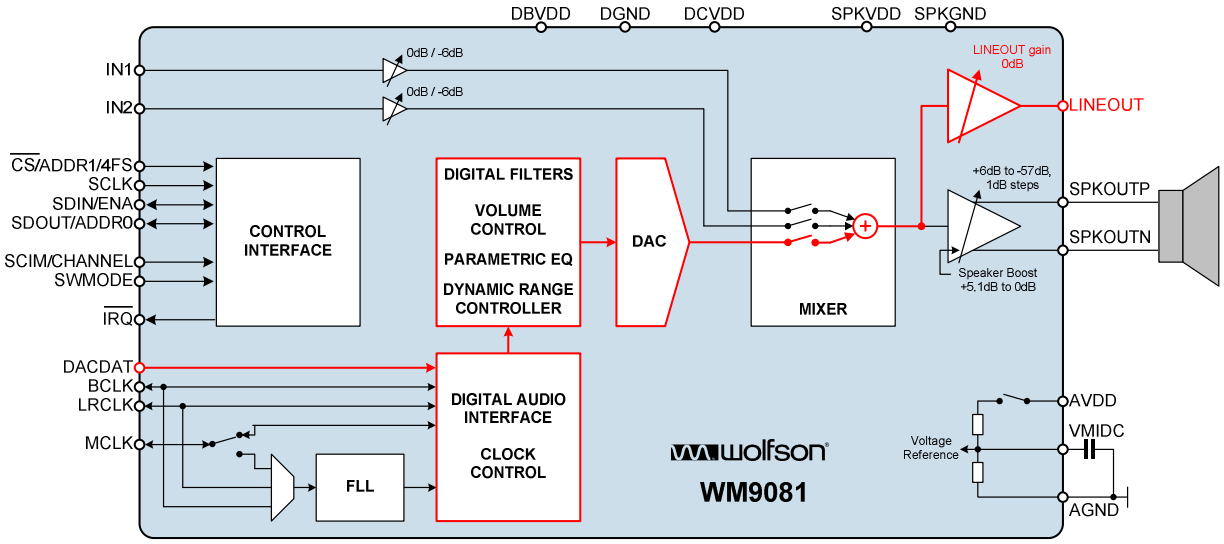

Figure 2 Signal Path: Sequence 3

STEP	REGISTER ADDRESS	BIT	DESCRIPTION
1	R8 (08h)	2	LINEOUT_DISCH = 1 Delay = 32ms
2	R4 (04h)	3:0	VMID_RAMP = 1 VMID_SEL [1:0] = 00 VMID_FAST_ST = 0
3	R5 (05h)	6:0	BIAS_SRC = 1 STBY_BIAS_LVL = 1 STBY_BIAS_ENA = 0 BIAS_LVL [1:0] = 10 BIAS_ENA = 1 STARTUP_BIAS_ENA = 1
4	R11 (0Bh)	4	LINEOUT_ENA = 1
5	R8 (08h)	2	LINEOUT_DISCH = 0
6	R4 (04h)	2:1	VMID_SEL [1:0] = 01 Delay = 512ms
7	R4 (04h)	3	VMID_RAMP = 0
8	R5 (05h)	6	BIAS_SRC = 0
9	R14 (0Eh)	1	CLK_DSP_ENA = 1
10	R11 (0Bh)	0	DAC_ENA = 1
11	R7 (07h)	4	DAC_SEL = 1
12	R2 (02h)	7	LINEOUT_MUTE = 0
13	R31 (1Fh)	10:3	DAC_MUTERATE = 1 DAC_MUTEMODE = 1 DAC_MUTE = 0 End of Sequence

Table 3 Sequence 3

4. LINEOUT DISABLE SEQUENCE

The Lineout disable sequence is initiated by writing 813Fh to Register 38 (26h). This single operation starts the Control Write Sequencer at Index Address 63 (3Fh) and executes the sequence defined in Table 4. For typical clocking configurations with MCLK=12.288MHz, this sequence takes approximately 646ms to run.

STEP	REGISTER ADDRESS	BIT	DESCRIPTION
1	R4 (04h)	3:0	VMID_RAMP = 1 VMID_SEL [1:0] = 01 VMID_FAST_ST = 0
2	R5 (05h)	6:0	BIAS_SRC = 1 STBY_BIAS_LVL = 1 STBY_BIAS_ENA = 0 BIAS_LVL [1:0] = 10 BIAS_ENA = 1 STARTUP_BIAS_ENA = 1
3	R31 (1Fh)	10:3	DAC_MUTERATE = 1 DAC_MUTEMODE = 1 DAC_MUTE = 1 Delay = 128ms
4	R2 (02h)	7	LINEOUT_MUTE = 1
5	R4 (04h)	2:1	VMID_SEL [1:0] = 00 Delay = 512ms
6	R11 (0Bh)	4	LINEOUT_ENA = 0
7	R7 (07h)	4	DAC_SEL = 0
8	R11 (0Bh)	0	DAC_ENA = 0
9	R14 (0Eh)	1	CLK_DSP_ENA = 0
10	R8 (08h)	2	LINEOUT_DISCH = 1
11	R4 (04h)	5:3	VMID_BUF_ENA = 0 VMID_RAMP = 0
12	R5 (05h)	1:0	BIAS_ENA = 0 STARTUP_BIAS_ENA = 0 End of Sequence

Table 4 Sequence 4

5. CLASS AB SPEAKER ENABLE SEQUENCE

The Class AB Speaker Enable sequence is initiated by writing 8154h to Register 38 (26h). This operation starts the Control Write Sequencer at Index Address 84 (54h) and executes the sequence defined in Table 5. For typical clocking configurations with MCLK=12.288MHz, this sequence takes approximately 42ms to run.

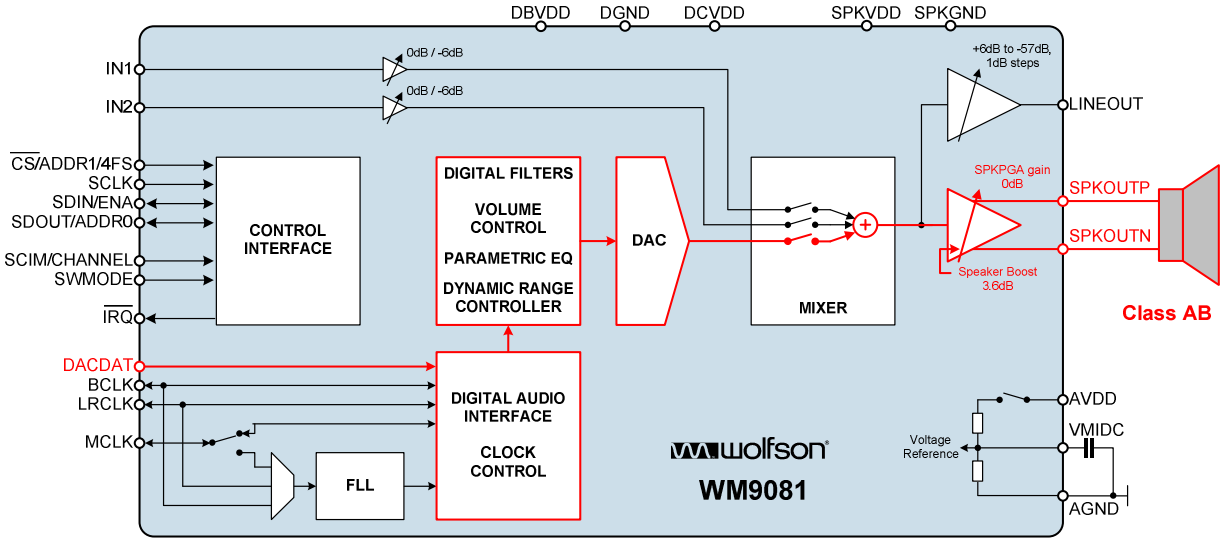

Figure 3 Signal Path: Sequence 5

Note that this sequence is optimized for pop suppression on the Speaker output. For pop suppression on the Line Output, please refer to sequence 3.

STEP	REGISTER ADDRESS	BIT	DESCRIPTION
1	R4 (04h)	3:0	VMID_RAMP = 1 VMID_SEL [1:0] = 00 VMID_FAST_ST = 1
2	R8 (08h)	2	LINEOUT_DISCH = 1
3	R11 (0Bh)	4	LINEOUT_ENA = 1
4	R8 (08h)	2	LINEOUT_DISCH = 0
5	R5 (05h)	6:0	BIAS_SRC = 0 STBY_BIAS_LVL = 1 STBY_BIAS_ENA = 0 BIAS_LVL [1:0] = 10 BIAS_ENA = 1 STARTUP_BIAS_ENA = 1
6	R10 (0Ah)	4:3	SPK_INV_MUTE = 0 OUT_SPK_CTRL = 0
7	R4 (04h)	2:1	VMID_SEL [1:0] = 01 Delay = 32ms
8	R4 (04h)	5:3	VMID_BUF_ENA = 1 VMID_RAMP = 0
9	R14 (0Eh)	1	CLK_DSP_ENA = 1
10	R11 (0Bh)	0	DAC_ENA = 1
11	R7 (07h)	4	DAC_SEL = 1
12	R10 (0Ah)	6	SPK_MODE = 1
13	R11 (0Bh)	2	SPKPGA_ENA = 1
14	R3 (03h)	7	SPKPGA_MUTE = 0
15	R11 (0Bh)	1	SPK_ENA = 1
16	R8 (08h)	0	LINEOUT_CLAMP = 1
17	R11 (0Bh)	4	LINEOUT_ENA = 0
18	R31 (1Fh)	9:3	DAC_MUTEMODE = 1 DAC_MUTE = 0 End of Sequence

Table 5 Sequence 5

6. CLASS AB SPEAKER DISABLE SEQUENCE

The Class AB Speaker Disable sequence is initiated by writing 8169h to Register 38 (26h). This single operation starts the Control Write Sequencer at Index Address 105 (69h) and executes the sequence defined in Table 6. For typical clocking configurations with MCLK=12.288MHz, this sequence takes approximately 49ms to run.

STEP	REGISTER ADDRESS	BIT	DESCRIPTION
1	R4 (04h)	3:0	VMID_RAMP = 1 VMID_SEL [1:0] = 01 VMID_FAST_ST = 1
2	R5 (05h)	0	STARTUP_BIAS_ENA = 1
3	R31 (1Fh)	9:3	DAC_MUTEMODE = 1 DAC_MUTE = 1 Delay = 8.5ms
4	R3 (03h)	7	SPKPGA_MUTE = 1
5	R11 (0Bh)	4:1	LINEOUT_ENA = 1 SPKPGA_ENA = 1 SPK_ENA = 0
6	R2 (02h)	7	LINEOUT_MUTE = 1
7	R8 (08h)	0	LINEOUT_CLAMP = 0
8	R4 (04h)	2:1	VMID_SEL [1:0] = 00 Delay = 32ms
9	R11 (0Bh)	4:2	LINEOUT_ENA = 0 SPKPGA_ENA = 0
10	R8 (08h)	2	LINEOUT_DISCH = 1
11	R7 (07h)	4	DAC_SEL = 0
12	R11 (0Bh)	0	DAC_ENA = 0
13	R14 (0Eh)	1	CLK_DSP_ENA = 0
14	R10 (0Ah)	6:3	SPK_MODE = 0 MIX_TO_SPK = 0 SPK_INV_MUTE = 1 OUT_SPK_CTRL = 1
15	R4 (04h)	3	VMID_RAMP = 0
16	R5 (05h)	1:0	BIAS_ENA = 0 STARTUP_BIAS_ENA = 0 End of Sequence

Table 6 Sequence 6

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