WAN_0207

Wolfson Control Write Sequencer

"The Control Write Sequencer is a function that executes pre-programmed sequences of register operations with a high degree of autonomy from the host processor. This means that time-critical configuration sequences may be initiated by a single instruction, simplifying product development and allowing the application processors to execute other functions while the sequencer takes care of highly sensitive operations such as pop & click suppression."

INTRODUCTION

- The Control Write Sequencer provides an instruction cache, which reduces application development effort and also enables efficient use of processor resources in the final product.
- Configuration of typical operating modes may require some 10-20 register writes; many of which may be time-critical for pop/click control.
- By reducing the dependency on the host processor, the sequencer delivers consistent implementation of the required control sequences through device evaluation, production prototyping and final production testing.

BACKGROUND

Wolfson CODECs are highly configurable and are typically controlled using control registers accessed via a serial interface. The Wolfson Control Write Sequencer provides a simple mechanism for executing complex sequences of control instructions.

The applications of the sequencer include functions such as power-up, power-down and signal path configuration; these should each follow a carefully designed sequence optimised for pop/noise performance and execution time.

The sequencer reduces product development time as the most common application requirements are provided as ready-programmed default operations. Minimal customisation may be needed for the wide range of configurations in complex 'audio hub' devices.

The sequencer reduces the workload of the CODEC host processor - a control sequence can be initiated and then left to run autonomously while the host is free to service other system requirements.

By simplifying the protocol for controlling the CODEC, migration to other Wolfson CODECs is also simplified - the same control instruction may be applicable to more than one device, and any differences in the implementation are managed within the CODECs rather than in the host processor.

DESCRIPTION

The Control Write Sequencer is controlled via the serial interface. The instruction sequences within the Write Sequencer memory are initiated by writing to specific register addresses as directed by the device datasheet.

The Register Map and Control Write Sequencer configuration of a typical device is illustrated in Figure 1. Commands and data can be written to the Control Write Sequencer via the main Register Map. The Control Write Sequencer modifies the Register Map according to the instructions stored within its RAM or ROM storage.

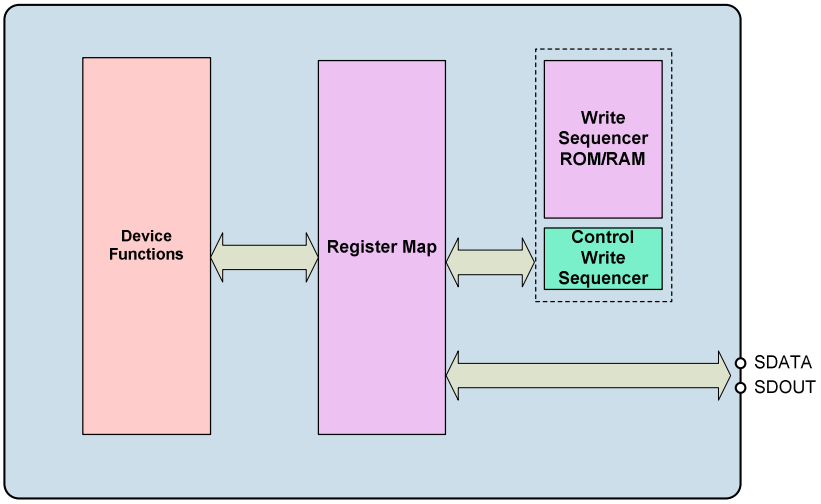

Figure 1 Register Map Control using Control Write Sequencer

When a control sequence is commanded, the Write Sequencer reads a sequence of commands from its memory bank. This memory bank is separate from the main register map.

Each command within the sequence comprises a data word to be written to a specified location within the main register map. The width of the data word, and the bit position within the main register map are configurable. This capability enables specific control bits to be written without affecting control fields at other bit positions within the same register address. The capability to write to specific bits within a data word is illustrated in Figure 2 for a portion of the WM8903 Register Map.

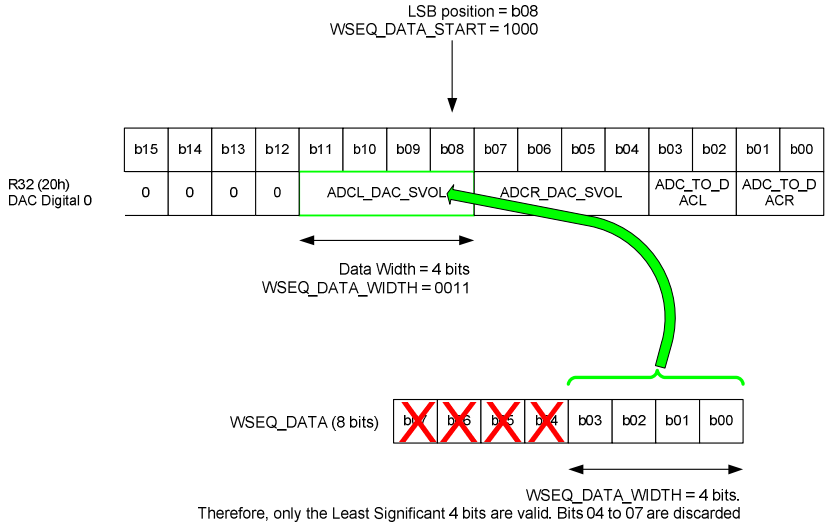

Figure 2 Register Map Control using Control Write Sequencer

Each step within the sequence takes a finite time to be executed. Additional delay times may be commanded at specific points in the sequence - for example, to allow a capacitor to charge or discharge before the next control step is scheduled. It should be noted that the timing of the register writes is frequently of crucial importance to the control sequence.

APPLICATIONS INFORMATION

The Wolfson WM8903 is an ultra-low power CODEC suitable for Portable Audio Applications. This device incorporates a Control Write Sequencer. Two default control sequences are provided - one for device Start-Up and one for device Shut-Down. Provided that the device clock (MCLK) is present and CLK_SYS_ENA is set, the Control Write Sequencer is ready to be instructed.

The WM8903 Default Start-Up sequence is scheduled by writing 0100h to Register 111 (6Fh). This single operation starts the Control Write Sequencer at Index Address 0 (00h), leading to a time-optimised sequence of 25 register writes. This provides a highly efficient control procedure, with minimum demands on the host processor.

Default sequences are provided on different devices which are specifically tailored to the requirements and applications of that device. For example, the WM9081 provides multiple sequences for selecting different signal paths and operating modes.

The application designer does not need to understand every available control bit, and does not need to study the differences from one CODEC to another in order to command the ready-programmed sequences.

The default sequences may be modified on some devices if required.

A typical application circuit using the WM8903 audio CODEC is illustrated in Figure 3. The CODEC is configured using the commands issued over the I2C control interface. Writing to the Control Write Sequencer in this way can initiate a sequence of register operations to power-up, power-down or re-configure the CODEC.

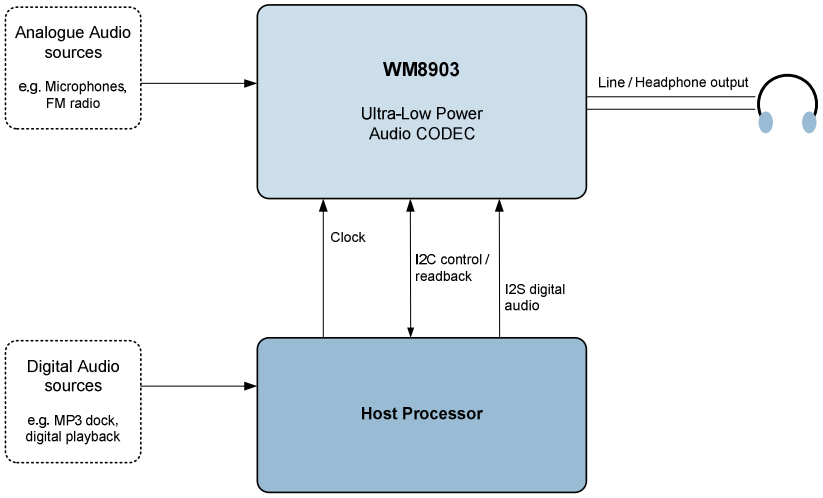

Figure 3 Typical Application for WM8903 Audio CODEC

APPLICABLE PRODUCTS

The Control Write Sequencer is currently incorporated within the devices listed below. Note that other devices may also be applicable, but may post-date this list.

- WM8903 – Ultra low power CODEC
- WM8993 - Multimedia CODEC
- WM9090 – Ultra low power audio subsystem
- WM9081 - 2W mono Class AB/D speaker driver

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