Wolfson Frequency Locked Loop (FLL)

"The Frequency Locked Loop is a versatile circuit which can generate a clock signal using frequency conversion from a reference source of a different frequency. This provides flexibility to interface with whatever clock source is available, and also to reconfigure the clock configuration under software control for different operating modes. It is similar to a PLL, but includes digital features to provide a higher degree of optimisation, by allowing control of parameters such as jitter and bandwidth."

INTRODUCTION

- The Frequency Locked Loop (FLL) generates the high quality system clock required by digital audio circuits. It provides compatibility with a wide range of reference clocks, including ones which are prone to jitter.

- The frequency conversion and digital filter capability of the FLL allow designers to use common clock signals throughout a system, leading to reduced component count, simplified board layout and a reduction in EMI issues.

- The flexibility of the FLL enables it to be re-configured in software according to changing operating requirements; for example, the clocking circuit might be optimised either for power saving or for best audio performance, according to the available power source or according to user preferences.

BACKGROUND

Digital audio systems require a reliable and accurate system clock in order operate correctly and to achieve the desired audio performance. A CODEC uses the system clock to derive the sampling rates of the ADCs and DACs and to manage the digital audio interface. The system clock may also be used to control a DC-DC converter or a Charge Pump for ground-referenced audio output. The system clock is used on Class D amplifier components to control the PWM circuits.

In some applications, the system clock will be input directly at the required frequency. In most cases, it is necessary to use circuits within the CODEC to apply filtering to the external input and to transform the frequency to one or more new clock signals according to the requirements of the audio system. This has traditionally been achieved using a Phase Locked Loop (PLL). The latest Wolfson devices use a Frequency Locked Loop (FLL), which employs a digital loop filter (where the PLL is analogue) in order to deliver greatly enhanced control loop performance and also low power consumption.

The on-chip capability to generate the required system clocks has the advantage of greater compatibility with host systems and also avoids noise problems that are associated with supporting high frequency signals on PCBs. The predominantly digital design of the FLL allows for a very compact implementation inside the device, and one that can be scaled down with the overall chip geometry.

A phase locked loop (PLL) is a closed-loop frequency control system that uses phase detection to compare its own oscillator output with a reference input and adjusts its oscillator in order to maintain a fixed relationship with the reference input signal. The fundamental components of a PLL are illustrated in Figure 1.
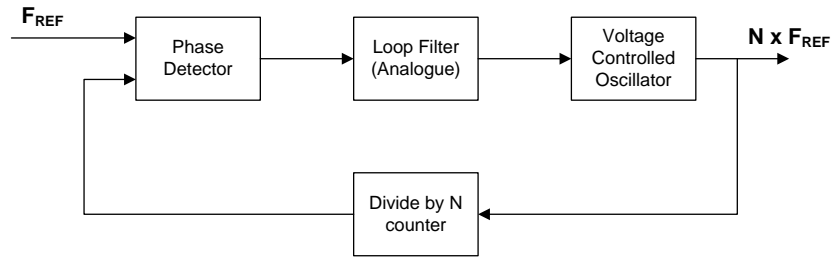
Figure 1 Phase Locked Loop Block Diagram

The Phase Detector measures the relationship between the PLL output and Reference input signals. The Phase Detector generates a signal that is a measure of the difference between its two inputs; the greater the frequency/phase difference in the two signals, the larger the output voltage.

The Loop Filter removes unwanted artefacts from the Phase Detector output, to improve the stability and noise characteristics of the control loop. Different circuit applications and different reference signal sources will demand different characteristics of this loop filter. If desired, the Loop Filter can be used to reduce the effects of short term irregularities in the reference and to ensure that the loop output settles on the desired average.

The Voltage Controlled Oscillator produces a locally generated clock, which is in fixed relationship to the input reference, but is otherwise independent of the input signal. In the case where a 1:1 frequency ratio is applied, the PLL can therefore generate a clean replica of the input signal, with a reduction in noise or jitter that may be present on the input reference.

Additional dividers and multipliers may be added to the configuration illustrated above in order to provide additional flexibility of input and output frequency ratios. With these additions, it is possible for the input reference to be multiplied or divided, by integers or real numbers, delivering a highly flexible capability to the circuit application.

Although it is possible to design a very high performance PLL, the jitter performance and power consumption tend to be inherently fixed at the design stage. In many applications, the ability to optimise and selectively adapt the clocking parameters for different modes of operation is a highly valuable feature. These are features that can be achieved with Wolfson's Frequency Locked Loop (FLL).

FREQUENCY LOCKED LOOP (FLL) DESCRIPTION

The main components of the Frequency Locked Loop are illustrated in Figure 2. It is similar in structure to the Phase Locked Loop already described. The digitally-implemented Loop Filter and Filter Control blocks enable a high degree of control to be exercised over the loop operation.

The Filter Control can be set and adjusted according to different application requirements (this is not possible in the case of the PLL). In a real application, the FLL may be adjusted any number of times and optimised specifically according to different needs (eg. to reflect the different needs of voice telephony compared with hi-fi audio).
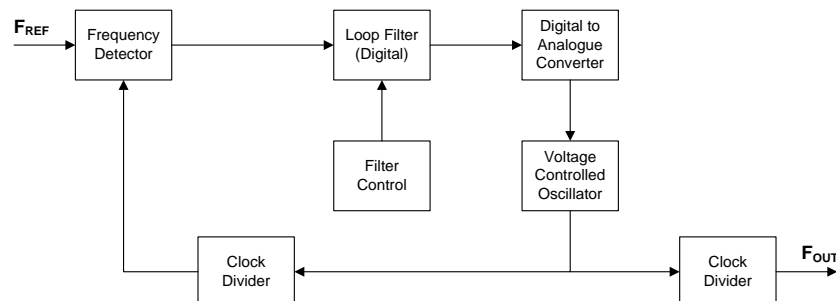

Figure 2 Frequency Locked Loop Block Diagram

In the FLL illustrated above, the Frequency Detector performs a similar task to the PLL's Phase Detector - it measures the relationship between the reference input signal and the output of the oscillator. The Frequency Detector measures the difference in frequency at its two inputs and generates an output that represents the ratio of these two frequencies. Programmable multipliers and dividers are implemented in order to support a very wide range of frequency ratios, whilst maintaining the VCO and Loop Filter control within their intended operating ranges.

The Loop Filter applies digital processing to the Frequency Detector output and to the VCO output in order to generate a digital control signal via the DAC to the VCO. These functions directly control the FLL output frequency.

The FLL's adaptive capability derives from the digital Loop Filter and Filter Control blocks. Adjustment of the loop 'gain' directly controls the loop 'bandwidth'. This parameter determines the stability of the loop frequency with respect to the reference frequency. A narrow bandwidth (low gain) results in the reference source being heavily filtered by the loop; this can be desirable in removing unwanted instabilities in the reference signal. A wide bandwidth (high gain) results in less filtering of the reference signal; this is appropriate where the reference frequency is highly stable or where the loop is required to adapt quickly to changes in the input reference.

The FLL also offers a user-adjustable loop 'control rate' parameter which determines the nature of the loop performance. Noise is present in the loop due, in part, to digital quantisation of the signal that feeds the DAC and VCO. Increasing the control rate results in a reduction in quantisation noise in much the same way as oversampled audio processing can reduce noise in ADC processes. Increasing the control rate, however, also increases the power consumption. By providing the facility to adjust the control rate, the FLL enables the power consumption to be optimised according to the actual SNR requirement for an application.

In summary, the FLL is a highly adaptive and programmable frequency synthesiser that can support a wide range of input/output frequency ratios. The input filtering, quantisation noise and power consumption are all adjustable, enabling the FLL to be optimised and adjusted for different applications and modes.

APPLICATIONS INFORMATION

The configuration of the FLL is described in the applicable device datasheet. In a typical device, control registers are provided to select the FLL input reference source, and also to enable the FLL output as the system clock.

Some devices support automatic configuration of the FLL, where a single register is set according to the FLL input reference frequency only. Other devices require the frequency ratios to be commanded using a small number of control registers. It is important that the FLL oscillator (VCO) is maintained within its recommended operating limits, as the performance falls off rapidly if this is not the case. The device datasheet contains the required information to configure the FLL for a wide range of input/output clock ratios.

The 'advanced' FLL control fields for loop gain / bandwidth and for setting the power / performance balance can either be set as recommended in the datasheet, or may be adjusted using practical in-circuit experimentation. Due to the complexity of the numerous parameters that can influence the CODEC performance, the FLL performance fields can only be optimised using a practical evaluation of the CODEC behaviour under different FLL settings.

For the purposes of adjusting the FLL parameters, it is recommended that the CODEC behaviour is assessed by measuring the SNR and THD+N characteristics of a 19kHz test tone. This frequency, at the high end of the audio frequency range, is chosen because clock jitter will have a greater impact on high frequencies than on lower frequencies.

To optimise the power consumption for a given level of performance, it is recommended to start with the fastest setting of Control Rate, and to adjust this field step by step until the SNR or THD+N of the circuit is compromised. The optimum setting is the slowest setting at which the audio performance is still acceptable for the application. Alternatively, if power consumption is not important, it is recommended to use the fastest Control Rate setting.

The most appropriate setting of the Loop Gain depends upon the stability of the input clock reference, as described below:

Selecting the lowest gain setting will result in a narrow loop bandwidth. This will heavily filter the input clock reference, meaning that the effects of an unstable clock source are minimised. If the external reference is of poor or unknown quality, then a low gain setting is recommended in order to achieve a stable output from the FLL. However, if the external reference is of high quality, then the low gain setting is not ideal and the FLL output will be sub-optimal due to jitter arising from the FLL itself.

Selecting a higher gain setting will result in a wide loop bandwidth and the lowest level of intrinsic (FLL) jitter. If the input clock reference is of high quality, then a higher gain setting is preferred for this reason. The high gain setting results in the minimum filtering of the external reference, which is not a concern if the input clock reference is of high quality. However, if a high gain setting is used with a poor quality clock source, this will result in poor ADC/DAC performance as the reference clock jitter will be present in the ADC/DAC clocking circuits.

Increasing the gain setting above the minimum may improve the audio performance provided that the input clock reference is of high quality. If the reference is not of high quality, then increased gain will degrade the audio performance. Note that excessive gain may lead to unstable FLL operation, even in the case of a high quality input clock reference.

APPLICABLE PRODUCTS

The Frequency Locked Loop is incorporated within the devices listed below. Note that this is not an exhaustive list. Note also that other devices may also be applicable, but may post-date this list.

- WM8900 - Ultra-low power CODEC
- WM8904 - Ultra-low power CODEC
- WM8993 - Multimedia CODEC
- WM8350, WM8351, WM8352 - Stereo CODEC with power management
- WM8400 - Stereo CODEC with power management

APPLICATION SUPPORT

If you require more information or require technical support, please contact the Wolfson Microelectronics Applications group through the following channels:

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or contact your local Wolfson representative.

Additional information may be made available on our web site at:

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