WAN_0276

WM8962 to WM8962B Migration Document

INTRODUCTION

The WM8962B is a new device succeeding the WM8962. The WM8962B is completely backwards compatible and includes several functional improvements.

This document outlines differences between the WM8962 and WM8962B.

CHANGE LOG

The changes between the WM8962 and WM8962B are summarised in the table below.

	FEATURE	WM8962	WM8962B
1	Reported Device Revision	011b	101b
2	Oscillator to MCLK path	FLL or PLL must be used to get MCLK from Oscillator.	MCLK can be provided by the Oscillator via a clock divider, without requiring an FLL or PLL to be enabled.
3	Higher MICBIAS Voltage Options	MICBIAS output voltage can be 0.84 x AVDD or 1.18 x AVDD.	MICBIAS output voltage can be 0.84 x AVDD, 1.18 x AVDD, 1.34 x AVDD or 1.63 x AVDD.
4	Stereo 2W Speaker Output	Supports up to 1W/Ch or 2W in mono output configuration.	Supports up to 2W/Ch output power into 4ohm loads.

Table 1 Summary of Changes between WM8962 and WM8962B

HARDWARE MIGRATION

PACKAGE

There are no differences between package dimensions of the WM8962 and WM8962B.

PACKAGE	PITCH	DIMENSIONS
49-ball W-CSP	0.5mm	3.594 x 3.984 x 0.7mm

Table 2 WM8962/WM8962B Package Details

BALL-OUT

There are no differences between ball-out on the WM8962 and WM8962B.

Figure 1 WM8962/WM8962B Ball-Out

EXTERNAL COMPONENTS

There are no differences between external components for the WM8962 and WM8962B.

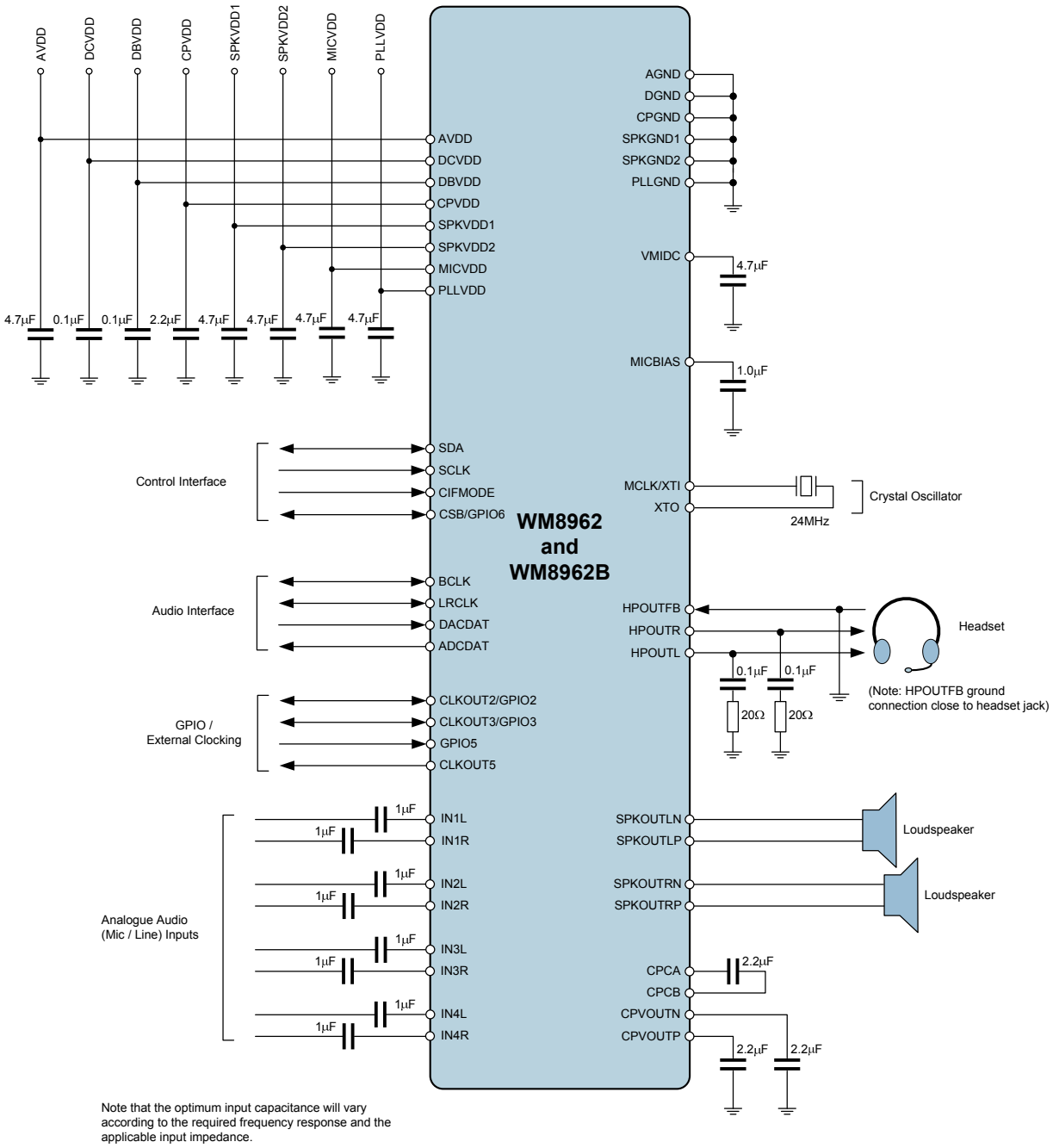

Figure 2 WM8962/WM8962B Recommended External Components

SOFTWARE MIGRATION

The WM8962B register map is fully backwards compatible with the WM8962 register map. When migrating from the WM8962 to the WM8962B, software changes will only be required where new features will be utilised.

The table below shows a cut down version of the register map, highlighting changes between the WM8962 and WM8962B. Any register fields or default register values that have been added or changed on the WM8962B are shaded grey with bold text. Default register values are shown on the far right-hand column.

Note that the changes to R01h will only affect read-back of this register,

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT WM8962	DEFAULT WM8962B
R01 (01h)	Right Input Volume	CUST_ID[3:0] (Read only)				**CHIP_REV[2:0] (Read only)**			IN_VU	INPGAR_MUTE	INR_ZC	INR_VOL[5:0]						0x069F	**0x0A9F**
R29 (1Dh)	Pwr Mgmt (3)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**MICBIAS_EVR [1:0]**		0x0000	0x0000
R152 (98h)	Analogue Clocking 4	0	0	0	0	0	0	0	0	1	1	0	**OSC_MCLK_SRC**	0	0	0	0	0x00C0	0x00C0

Table 3 Register Map Changes from WM8962 to WM8962B

Features that are new to the WM8962B are described in the following sections. More information about the new register map fields is also included in these sections.

1. REPORTED DEVICE REVISION

CHIP_REV can be read back from R01h[11:9] of the register map in the WM8962 and WM8962B. This value indicates the revision of the device. The WM8962 revision is 011b whilst the WM8962B revision is numbered as 101b.

2. OSCILLATOR TO MCLK PATH

On the WM8962, the internal oscillator must be used in conjunction with the FLL or PLL3 in order to be used as the MCLK source. On the WM8962B a new clock path is provided so that the oscillator can provide the MCLK source without having to enable the FLL or PLL3.

Figure 3 shows the internal clocking diagram for the WM8962B. The features highlighted in red are not available on the WM8962. The new multiplexor is controlled by OSC_MCLK_SRC.

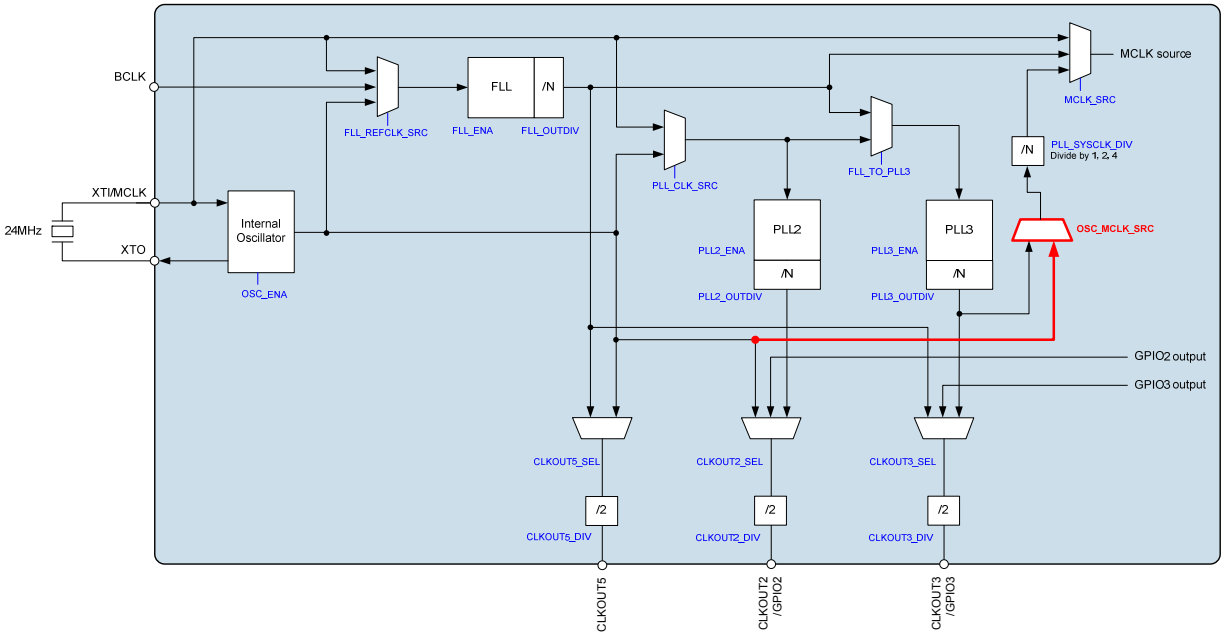

Figure 3 WM8962B Internal Clocking

The register control bit OSC_MCLK_SRC is described in the table below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R152 (98h) PLL Spare	4	OSC_MCLK_SRC	0	Oscillator or PLL3 MCLK source select 0 = PLL3 1 = Oscillator

Table 4 WM8962B OCS_MCLK_SRC

3. MICBIAS OUTPUT VOLTAGE

The WM8962 includes a configurable MICBIAS level controlled by MICBIAS_LVL. The WM8962B includes an additional register field, MICBIAS_EVR, which facilitates two further MICBIAS output levels.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Pwr Mgmt (1)	1	MICBIAS_ENA	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON
R29 (1Dh) Pwr Mgmt (3)	1:0	MICBIAS_EVR [1:0]	00	Microphone Bias Voltage Control 00 = Controlled by MICBIAS_LVL 01 = 1.59 x AVDD (approx.) 10 = 1.33 x AVDD (approx.) 11 = 1.59 x AVDD (approx.)
R48 (30h) Additional Control (4)	0	MICBIAS_LVL	1	Microphone Bias Voltage Control 0 = 0.828 x AVDD (approx.) 1 = 1.156 x AVDD (approx.) Only valid when MICBIAS_EVR=00. In other cases, the Microphone Bias voltage is controlled by MICBIAS_EVR alone.

Table 5 WM8962B MICBIAS Control

4. 2W SPEAKER OUTPUT POWER

The WM8962 supports up to 1W output power per channel into stereo 8Ω loads. The WM8962B supports up to 2W output per channel into stereo 4Ω loads.

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