A Cirrus Logic Company

AN90

Crystal LAN™
CS8904
Quad 10Base-T Ethernet Transceiver
Technical Reference Manual

Version: 1.0

AN90REV1

January 2, 1997

To obtain technical application support, call (800) 888-5016 (from the US and Canada)
or 512-442-7555 (from outside the US and Canada), and ask for CS8904 Application Support,
or send an email to: ethernet@crystal.cirrus.com

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http//www.crystal.com

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION TO THE CS8904 TECHNICAL REFERENCE MANUAL

This Technical Reference Manual provides information that will be helpful in designing a board using the CS8904 quad transceiver. It is expected that the user of this technical reference manual will have a general knowledge of hardware design and Ethernet. Recommended sources of background information are:

a) IEEE Std 802.3u-1995 (ISO/IEC 8802.3:1996) CSMA/CD Access Method and Physical Layer Specifications

b) IEEE Std 802.3u-1995 Supplement Clause 28 (Auto-Negotiation)

c) Ethernet, Building a Communication Infrastructure, by Hegering and Lapple, Addison-Wesley, 1993, ISBN 0-201-62405-2

d) Netware Training Guide: Networking Technologies, by Debra Niedenmiller-Chaffis, New Riders Publishing, ISBN 1-56205-363-9

1.0 Typical Installation

This section describes an example CS8904 implementation operating from a +5.0V power supply and using single-port RJ-45 connectors and magnetics.

1.1 Evaluation Board Schematics, Bill of Materials, and Layer Plots

Figures 1 through 7 show the schematic for the CDB8904-1 evaluation board. Figures 8 through 12 contain the layer plots of the 4-layer board. Table 1 lists the bill of materials used.

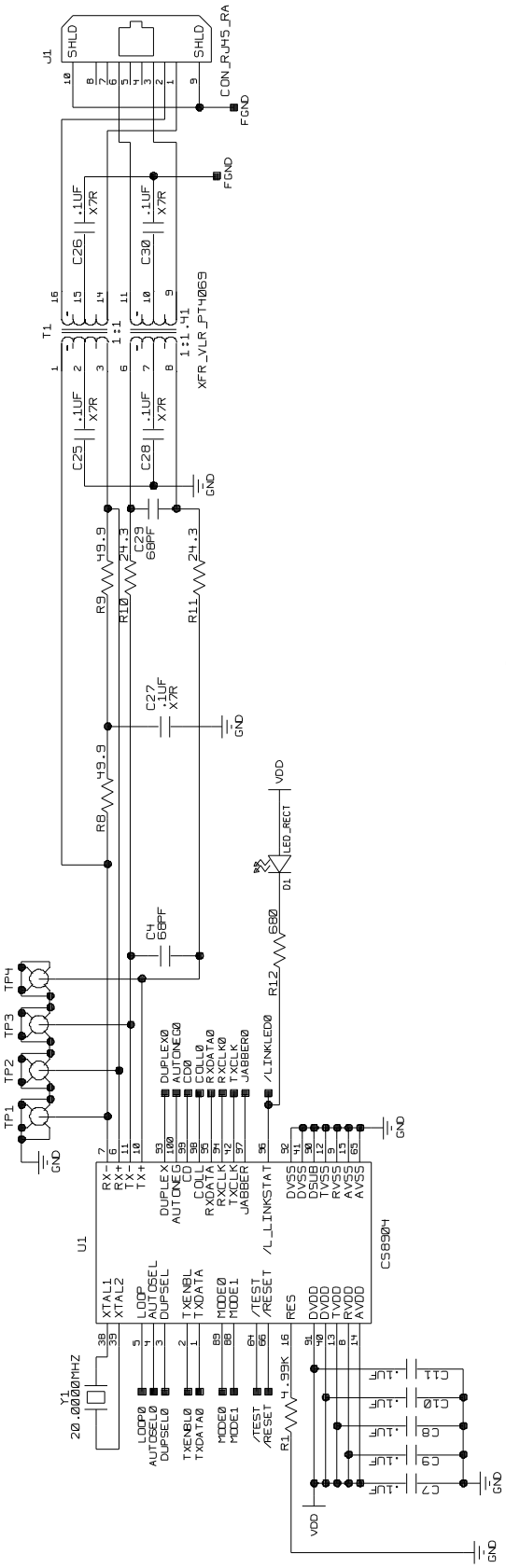

Figure 1. Port 0 Schematic

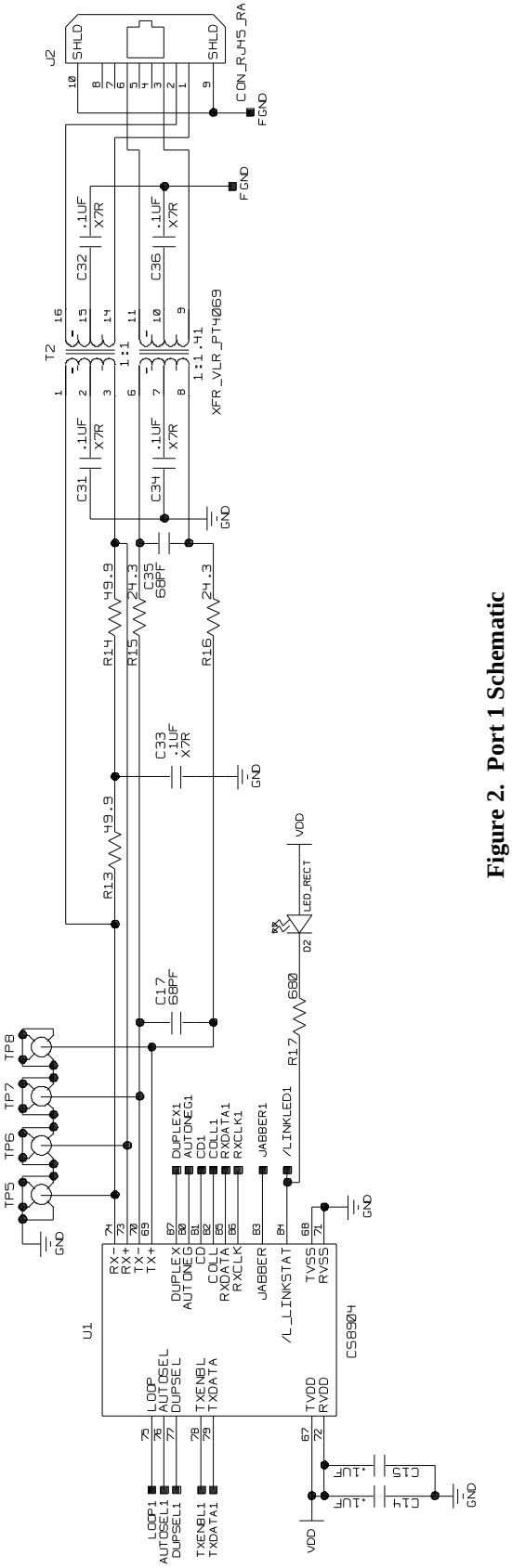

Figure 2. Port 1 Schematic

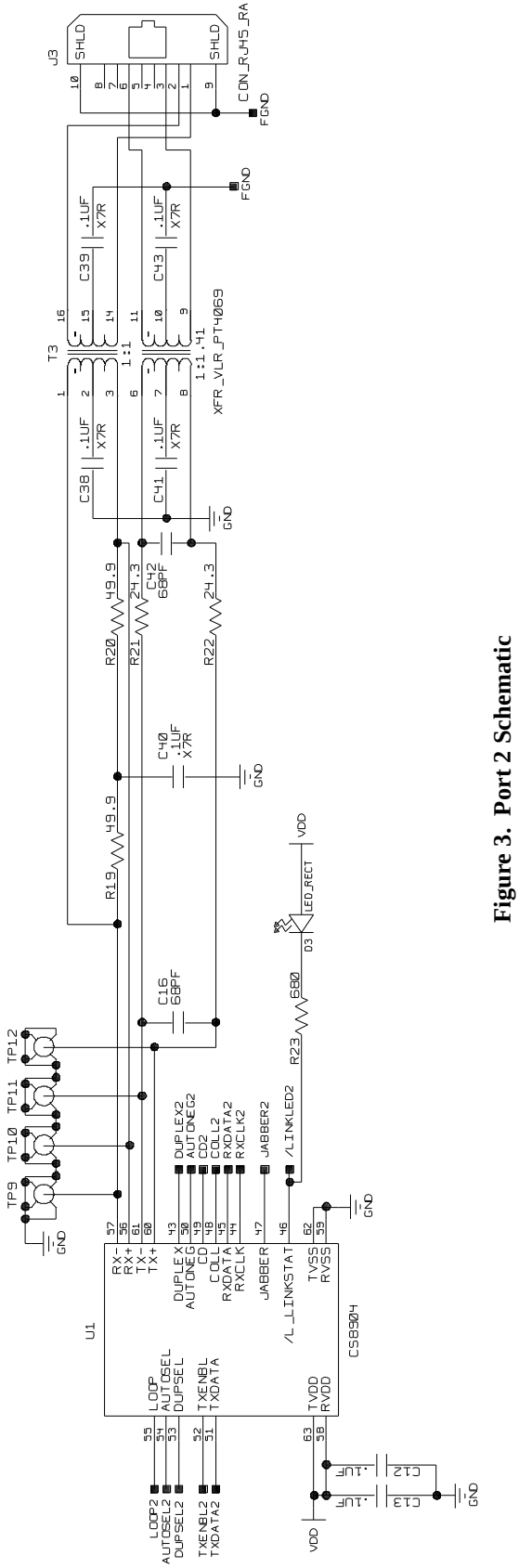

Figure 3. Port 2 Schematic

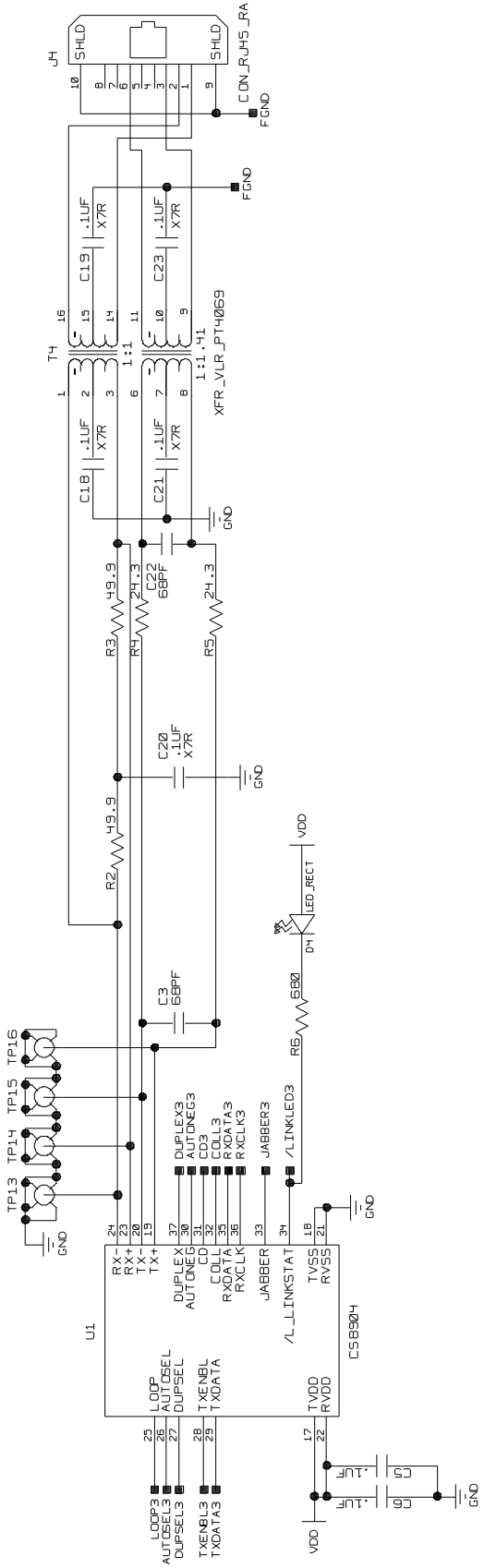

Figure 4. Port 3 Schematic

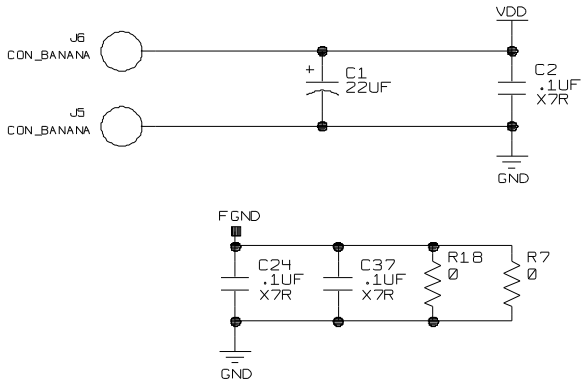

Figure 5. Power Supply Connections

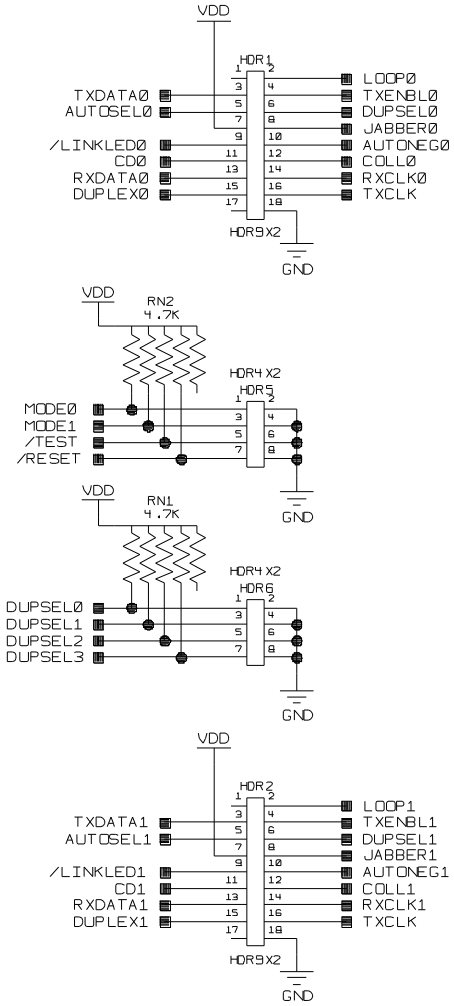

Figure 6. Header Schematic (1 of 2)

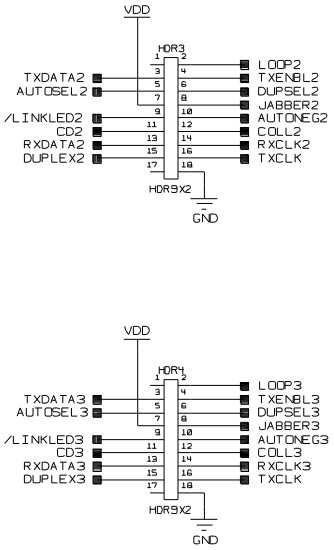

Figure 7. Header Schematic (2 of 2)

Item	Reference #	Description	Qty	Vendor	Part Number
1	C5..C15	Capacitor, 0.1µF, SMT 0805, X7R	11	NIC	NMC0805X7R104K2
2	C22, C29, C35, C42	Capacitor, 68pF, C315	4	Kemet	C315C680J2G5CA
3	C1	Capacitor, 22µF, T350K	1	Kemet	T350K226K035AS
4	C2, C20, C27, C33, C40	Capacitor, 0.1µF, C320	5	Kemet	C320C104K5R5CA
5	R4, R5, R10, R11, R15, R16, R21, R22	Resistor, 24.3, 1%, 1/8W, TH	8	Transohm	271_24.3
6	R2, R3, R8, R9, R13, R14, R19, R20	Resistor, 49.9, 1%, 1/8W, TH	8	Transohm	271_49.9
7	R6, R12, R17, R23	Resistor, 680, 5%, 1/8W, TH	4	Transohm	271_680
8	RN1, RN2	Resistor, 4.70k, SIP	2	Bourns	4606X_101_472
9	R1	Resistor, 4.99k, 1%, 1/8W, TH	1	Transohm	271_4.99K
10	D1..D4	LED	4	DiaLight	561-2201-050
11	Y1	Crystal, 20.000MHz	1	M-Tron	ATS-49
12	J1..J4	Connector, RJ45, 8 pin	4	AMP	55164-1
13	T1..T4	Transformer, 2, 1:1, 1:1.41 - DIP	4	Halo	TD42-2006Q
14	HDR1..HDR6	Header Strips	44	AMP	4-102973-0
15	J5	Banana Jacks	1	Voltrex	3-881-BK (Black)
16	J6	Banana Jacks	1	Voltrex	3-881-R (Red)
17	U1	Ethernet Controller	1	Crystal	CS8904
*	C3, C4, C16, C17	Capacitor, 68pF, C315	0		
*	C18, C19, C21, C23..C26, C28, C30..C32, C34, C36..C39, C41, C43	Capacitor, 0.1µF, C320	0		
*	R7, R18	Resistor, 0 ohms, TH	0		

* Not Loaded

Table 1. EEB8904 Bill of Materials

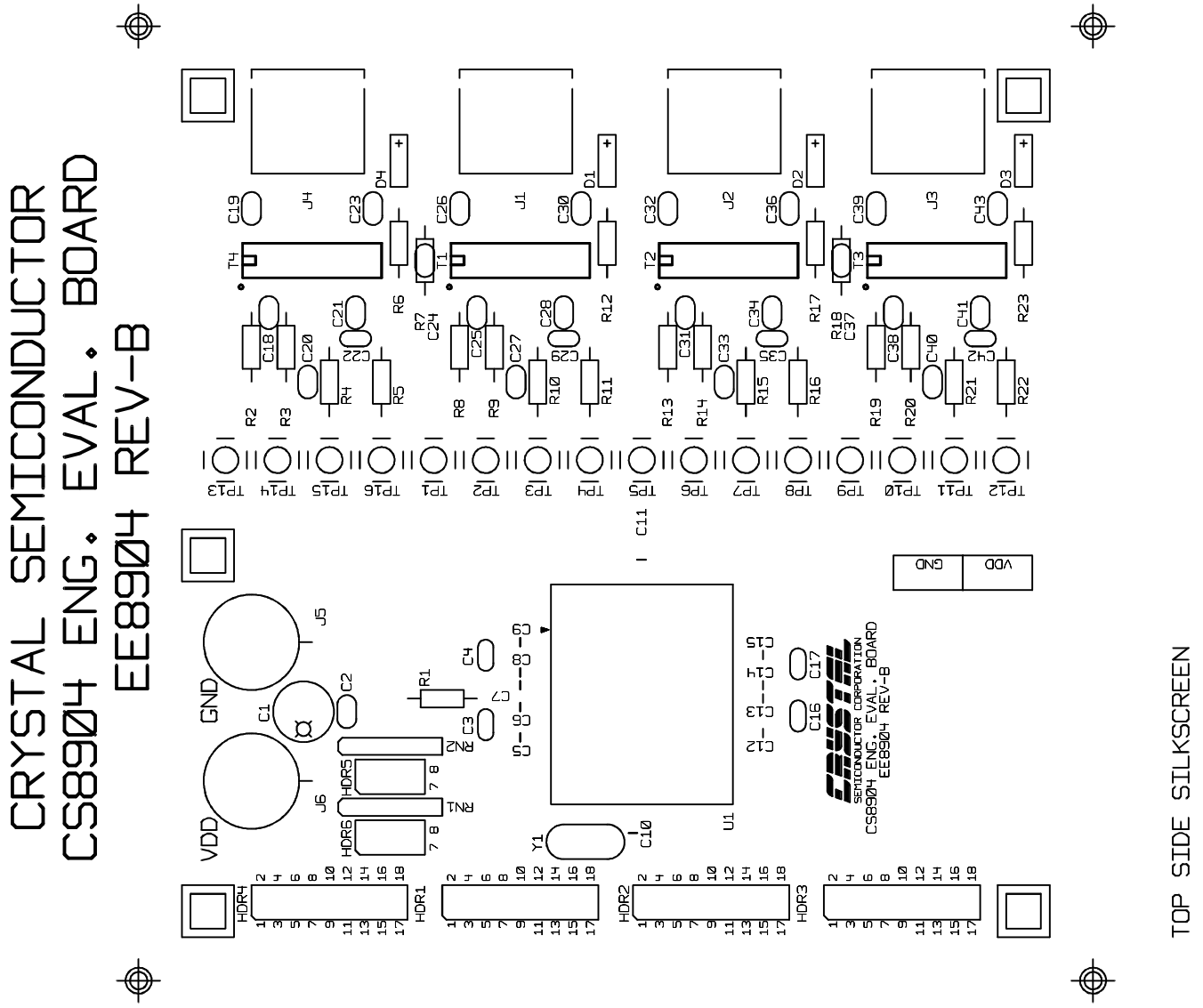

Figure 8. EEB8904B Silkscreen

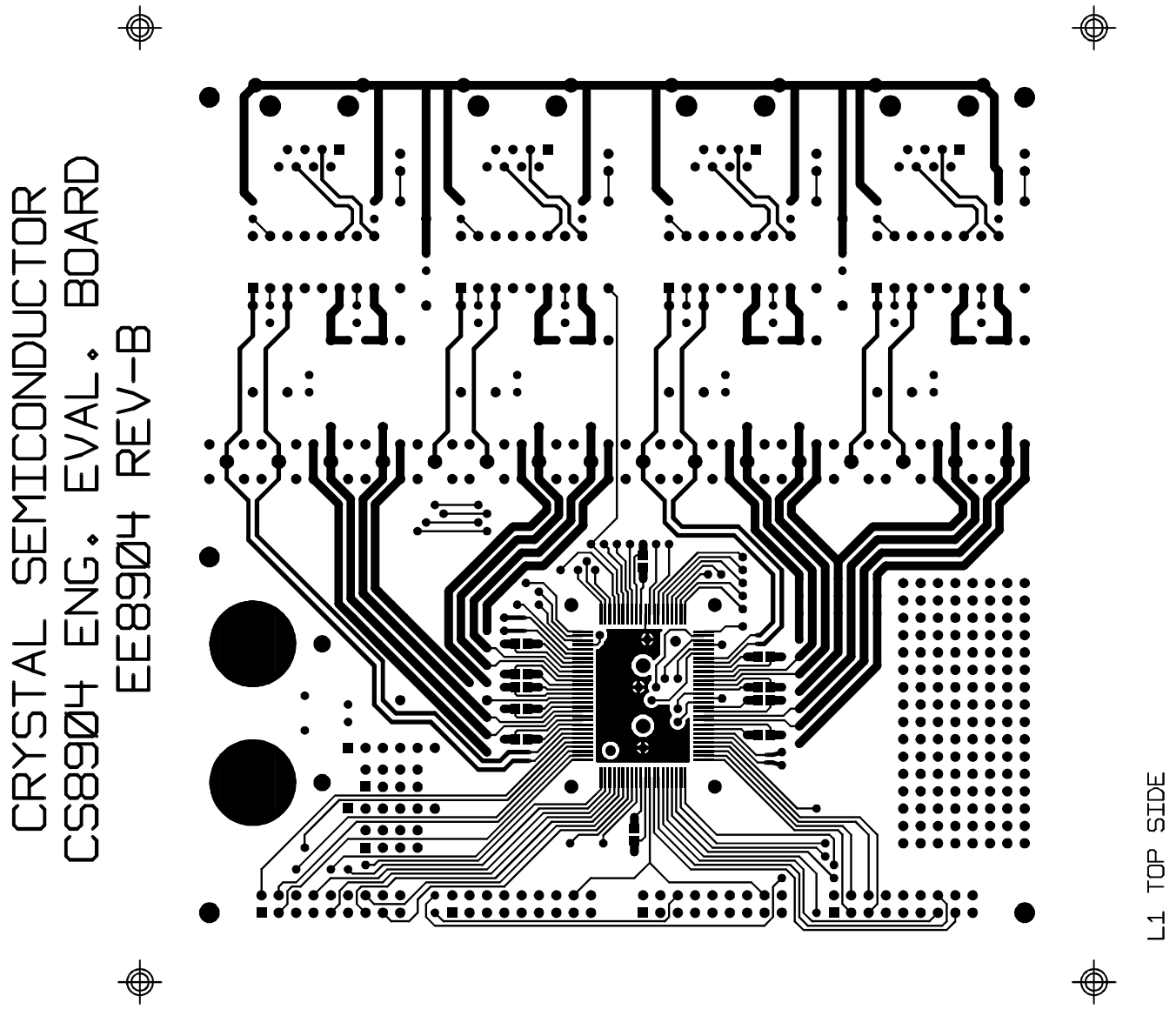

Figure 9. EEB8904B Component Side

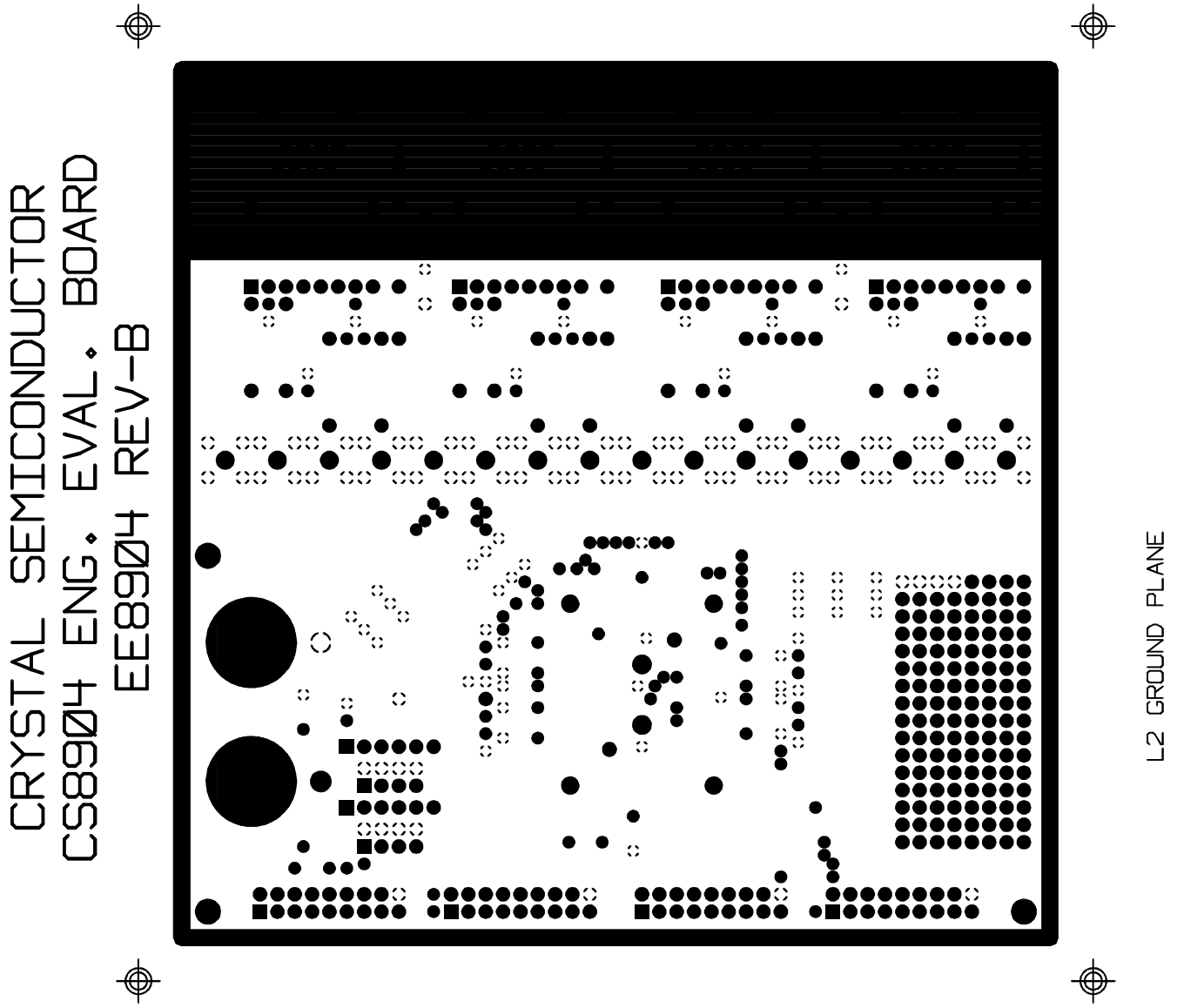

Figure 10. EEB8904B Ground Plane

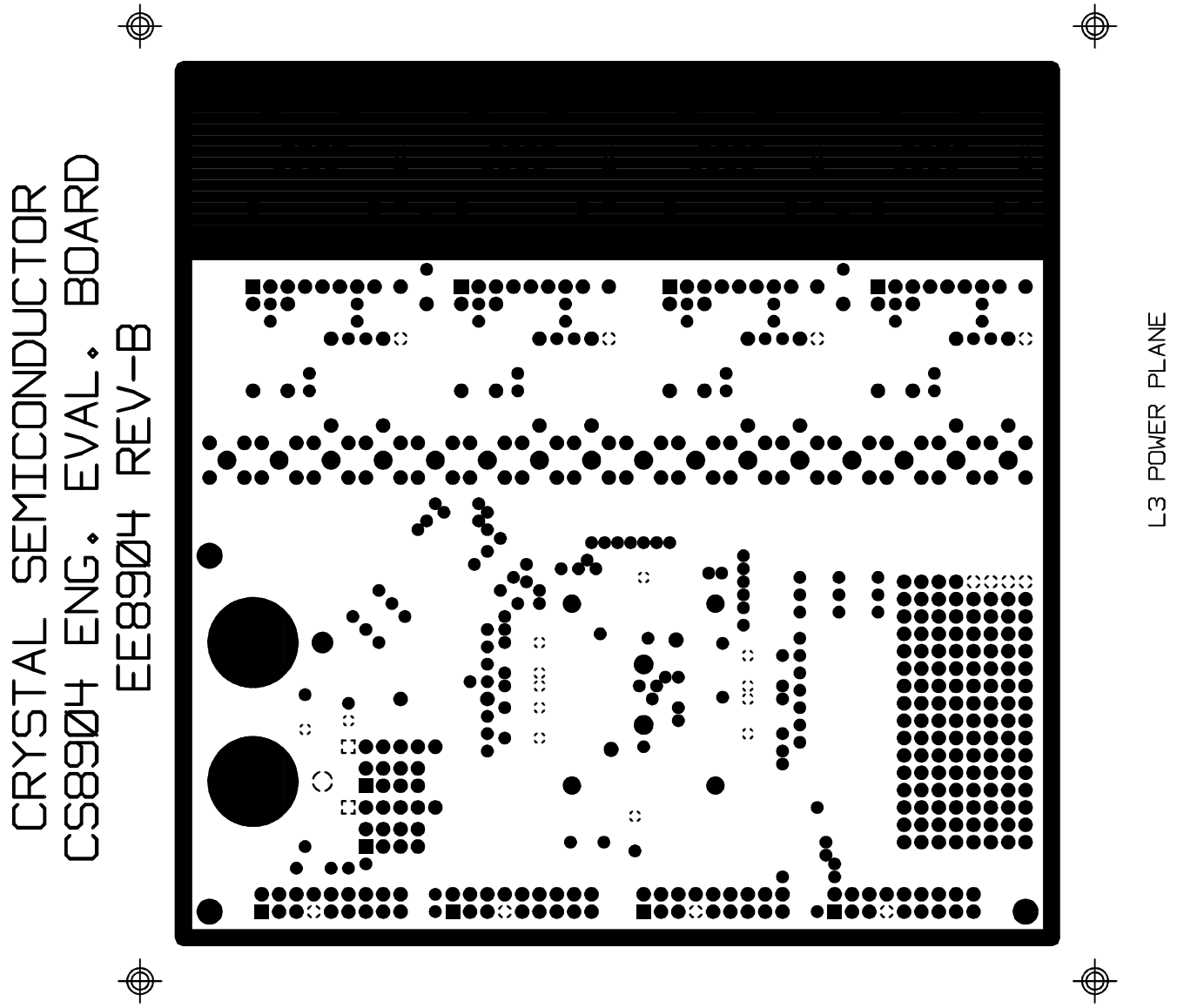

Figure 11. EEB8904B Power Plane

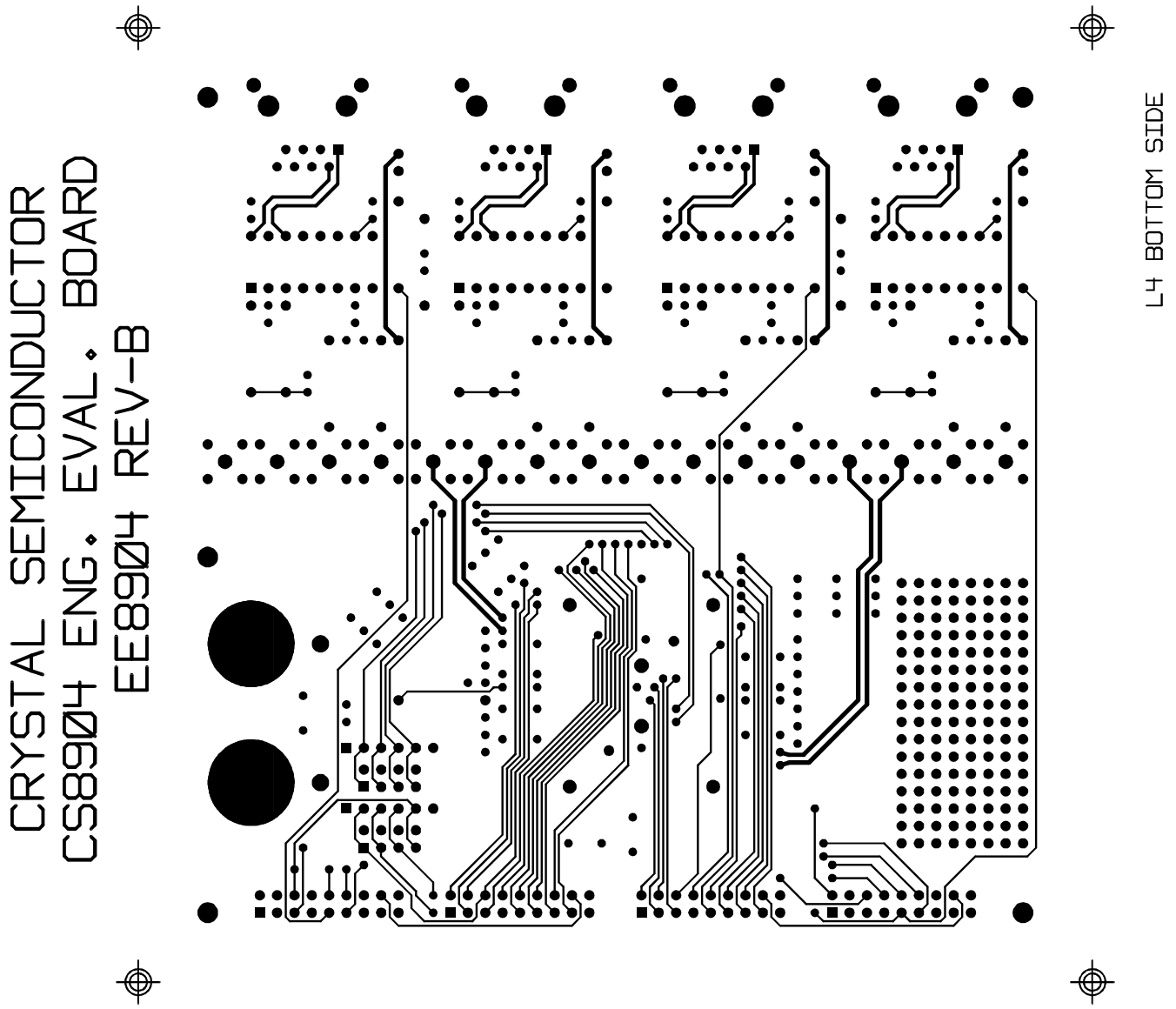

Figure 12. EEB8904B Solder Side

1.2 Crystal Oscillator

The clock to the CS8904 can be supplied by either a crystal or an external CMOS/TTL clock source. The crystal specifications are given in Table 2. The crystal should be connected between XTAL1 and XTAL2 (Pins 38 and 39 respectively) and should be placed as close as possible to the CS8904. If an external clock is used, it should be driven into XTAL1 (Pin 38), and XTAL2 (Pin 39) should be left floating (no connection).

1.3 LED Drivers

The CS8904 has 4 LED drivers, one per port, to indicate Link Status. These are open-drain outputs. Figure 13 shows a typical LED implementation. In this example, when a link has been established, the CS8904 LED driver turns on, allowing current to flow in the LED/resistor chain, thus activing the LED. When the link is disconnected, the driver turns off, cutting the current through the LED.

The use of an LED is optional. In systems that require use of the $\overline{\text{LINKLEDx}}$ signal, an external pull-up resistor is required. This signal is active low, that is, the output drives to a low voltage when the link is good.

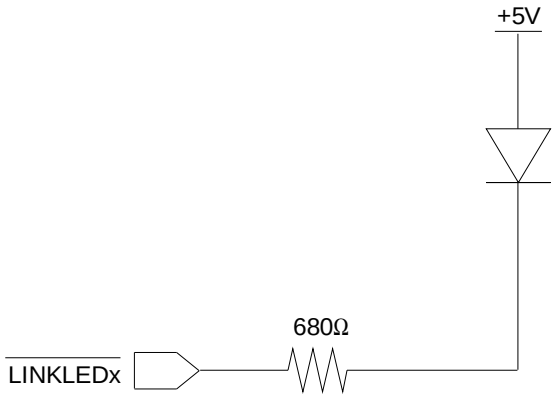

Figure 13. LED Circuit

1.4 10Base-T Interface

Figure 14 shows a typical 10Base-T interface. Transmit and receive lines from the CS8904 are routed to the RJ-45 jack through an isolation transformer. For +5.0V systems, this transformer has a turns ratio of 1:1 between the primary and secondary windings on the receive side (Rx+, Rx-) and 1:1.41 between the primary and secondary windings on the transmit side (Tx+, Tx-). A list of recommended transformers is given in Section 3.0.

In Figure 14, the 0.1µF capacitors provide for common-mode filtering on the transmit and receive coils. The Rr resistors provide for impedance matching on the receive lines. The Rt resistors and the Ct capacitor provide impedance matching for the transmit lines.

Parameters	Min	Typ	Max	Units
Parallel Resonant Frequency	-	20	-	MHz
Resonant Frequency Error (C_L = 18 pF)	-50	-	+50	ppm
Resonant Frequency Change over Operating Termperature	-40	-	+40	ppm
Crystal Capacitance	-	-	18	pF
Motional Crystal Capacitance	-	0.022	-	pF
Series Resistance	-	-	35	Ω

Table 2. Crystal Oscillator Requirements

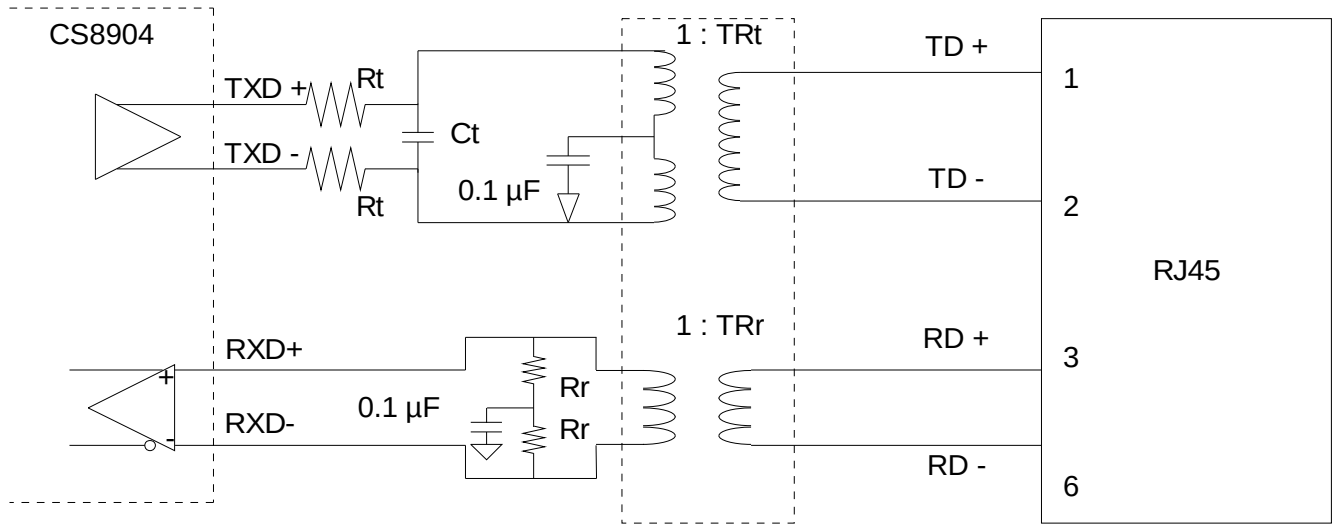

Figure 14. 10Base-T Interface Circuit

2.0 +3 V Operation

When the CS8904 is operating from a +3.0V power supply, the 10Base-T interface is modified slightly. Namely, the turns ratio between the primary and secondary windings on the transmit isolation transformer must be changed from 1:1.41 to 1:2.5. The turns ratio between the primary and secondary windings on the receive side remain 1:1. Additionally, the values for the impedance matching components change as well. These changes are summarized in Table 3.

Parameter	+5.0 V	+3.0 V
TRt	1:1.41	1:2.5
TRr	1:1	1:1
Rr	49.9 Ω	49.9 Ω
Rt	24.3 Ω	8 Ω
Ct	68 pF	560 pF

Table 3. 10Base-T Components for +5.0V and +3.0V Operation

3.0 Transformer Recommendations

Table 4 lists manufacturers and part numbers for transformers suitable for use with the CS8904 in +5.0V systems.

Vendor	CMC?	Through-hole	Surface-mount
Single-Port Transformers			
Halo	N	TD42-2006Q	TG42-1406N1
	Y	TD43-2006K	TG43-1406N
Pulse	N	PE-65994	PE-65745
	Y	PE-65998	PE-65746
Valor	N	PT4069	ST7011
	Y	PT4068	ST7010
Quad-Port Transformers			
Halo	N		TG44-1406NX
	Y		TG46-1406NX
Pulse	N		PE-68065
	Y		PE-68062
Valor	N		ST4212-1
	Y		ST4212-2

Table 4. Recommended Transformers

4.0 Using Multiple CS8904s with a Shared TxCLK

When the connecting a set of CS8904s to a MAC having a single TxCLK input, some design considerations must be met:

1. All CS8904s must operate from the same clock source.
2. A shared hardware RESET signal must be applied to all CS8904's after power-up.
3. The TxCLK signal should be taken from exactly one CS8904 and routed to the TxCLK input on the media access controller. TxCLKs on the other CS8904's should be left unconnected.

5.0 Unused Ports

Ports that are not used in the system (those that have no external RJ-45 connection) should be configured as follows:

1. LOOPx should be asserted (polarity depends on MODE pins).
2. TxENBLx should be deasserted (polarity depends on MODE pins).
3. AUTOSELx, DUPSELx, and TxDATAx should all be tied high.
4. Tx+/Tx- should be left floating (no connection).
5. Rx+/Rx- should be tied together.

6.0 Layout Considerations

The CS8904 is a mixed-signal device, that is, it implements both sensitive analog circuitry and digital control and preprocessing circuitry on a single chip. The mixed-signal nature of the device makes it sensitive to component placement and routing. Below is a checklist of guidelines system designers should follow in laying out a printed circuit board.

6.1 Clock

- ❏ If the clock is supplied by an 20 Mhz crystal, that crystal should be placed on the component side of the board close to XTAL1 and XTAL2 (within one inch). Crystal traces should be short and should contain no vias.

  If the clock is supplied by an external CMOS/TTL source, the traces should be as short as possible.

6.2 Analog Signals

- ❏ The 4.99 KΩ biasing resistor should be placed close to pins 15 (AVSS0) and 16 (RES). The connection between the biasing resistor and AVSS0 should be made with a short trace.
- ❏ The isolation transformers should be placed as close as possible to the RJ-45 connectors. If common-mode chokes are employed, they must be placed on the RJ-45 side of the isolation transformers.
- ❏ Traces in the 10Base-T signal path, those leading from Rx+/Rx-, Tx+/Tx- on the CS8904 through the isolation transformer and out to the RJ-45 jack, should be direct and short. The trace width on the receive traces should be at least 25 mills (50 Ω characteristic impedance at 10 Mhz) and the trace width on the transmit traces should be at least 100 mills wide (25 Ω characteristic impedance at 10 MHz).

  Particular care should be taken to match the characteristic impedance of each transmit trace to the value of Rt (in Figure 14). For a +5.0V, 2-layer board using FR-4 laminate with a thickness of 0.0625", two 100 mill traces w/ ground plane underneath yield a characteristic impedance that approximately matches Rt.
- ❏ Route each differential signal pair for the transmit lines and the receive lines adjacently. For example, the trace leading from Rx+ should be routed parallel to the trace leading from Rx-. Additionally, special care should be taken to ensure that these traces have the same length.
- ❏ Add either "ground shield" traces or use ground

plane fill around each transmitter's differential signal pair. For example, the traces GND, Tx+, Tx-, GND, form a shielded differential signal pair. If the ground shield traces are used, they should be 'stitched', or tied to the groundplane periodically along their length. Figure 9 shows an example of using ground shielding traces on the transmit lines. The use of ground plane fill on all trace layers is strongly recommended.

6.3 Digital Signals

- ❏ Digital signals, particularly the MAC data signals (RxCLK, RxDATA, CD, TxCLK, TxDATA, TxENBL), should not be routed under the CS8904 and should be kept as far as possible from the analog traces.

6.4 Power

- ❏ Each power supply pin should be decoupled by its own small-valued (0.1µF or 0.01µF) decoupling capacitor. Each of these capacitors should be placed as close as possible to the power supply pins they decouple. Power supply traces, as well as traces to the decoupling capacitors, should typically be as wide as possible