Errata: CS8952 - Silicon revision: F

Reference CS8952 Data Sheet revision DS206PP3 dated October 2001.

Link Status Change Interrupt

Description

The datasheets for the CS8952 and CS8952T state that an interrupt can be generated on a link status change. This is true for 100 Mbps mode.

However, when operating the device in 10 Mbps mode, the *Link Status Change* interrupt mask bit (reg 0x10, bit 14) is effectively stuck at 0, thus preventing an interrupt from being generated whenever the link status changes. The status bit for this condition is still valid, as is the *Link Good LED* signal ($\overline{\text{LED3}}$).

Workaround

1) **Interrupt-driven System:** Use the *Link Good LED* signal ($\overline{\text{LED3}}$) along with additional interrupt-on-change logic to trigger an interrupt in the host whenever the link status changes.

2) **Polling-driven System:** Poll the *Link OK* bit in the *Self Status* register (reg 0x19, bit 15).