

Errata: CS42528 Rev. D

(Reference CS42528_DS586F1 Data Sheet)

All references to the CS42528 mentioned below shall be taken to refer to revision D of the CS42528 product. The hardware revision code can be found in the 10-character field printed on the last line below the part number of each chip. The letter that appears as the third character from the left is the revision code (e.g. WADXA0425 is a Revision D part).

- ◆ PLL locking to SAI_LRCK is not operational. The PLL_LRCK bit (register 06h, bit 3) must be set to '0'.
- ◆ With $V_D = 3.3\text{ V}$, S/PDIF receiver operation is limited to sample rates from 30 kHz to 100 kHz. With $V_D = 5\text{ V}$, the S/PDIF receiver will operate over the entire specified sample rate range (30 kHz to 200 kHz).
- ◆ When reading from or writing to the control port, the memory address pointer (MAP) will always automatically increment regardless of the setting of the INCR bit (the MSB of the 8-bit MAP).

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest you, go to <http://www.cirrus.com>