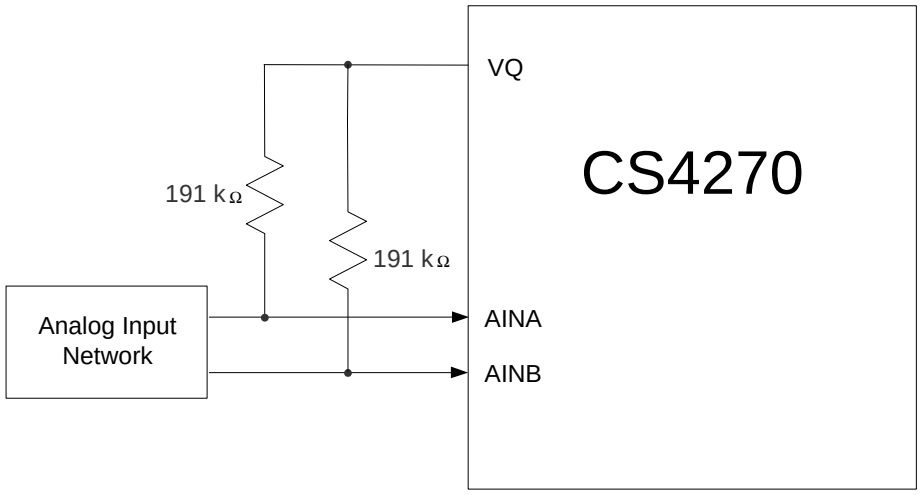
Errata: CS4270 Rev B0 Silicon

Reference CS4270 Data sheet DS686A1

- The common mode voltage at pins AINA and AINB rises over time after power up unless the pins are forced to the proper level by a 200 kΩ pull-up to the VQ pin where VQ = 2.5 V for VA = 5 V or VQ = 1.65 V for VA = 3.3 V. If the common mode voltage is not forced to VQ via a pull-up, the result will be clipping, increased distortion and degraded performance as seen at the A/D output.



- Measured DAC THD+N (0 dB) with VA = 5 V or 3.3 V could be -81 dB and does not meet the -89 dB max. specification in the Data Sheet.
- Measured DAC THD+N (0 dB) with VA = 3.0 V (3.3 V min.) is -79 dB and does not meet the -89 dB max. specification in the Data Sheet.
- In Control Port or Hardware modes, if the serial data format for SDOUT is changed, the phase match between the two channels in the serial bit stream will be off by 1 frame. A part power down/up (PDN) or resync condition (like remove/reapply LRCK) corrects the problem.
  - In Control Port mode, the part PDN bit (register 02h bit 0) should be cycled high then low after changing the serial data format when operating in Software mode.
- If the DAC mute on zero crossings option is set and the mute is asserted, occasionally the mute will occur either before or after the zero crossing. If proper mute/unmute on zero crossings is desired, first set the DAC Volume Control Register (07h or 08h) value to FFh then assert DAC mute.
- If the chip PDN bit (register 02h bit 0) is not set prior to entering control port mode, the ADCs may continuously output bad data on SDOUT. To avoid this problem, set the PDN bit to “1” (register 02h bit 0) to initiate control port communications and then set the PDN bit to “0”.

Contacting Cirrus Logic Support
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- Glitches or double edges on the MCLK after part power up can corrupt the ADC RAM internal to the part. The user should correct this MCLK condition if it exists and then apply a “hard reset” or cycle power to the part.
- The digital portions of the part (both ADC and DAC) will not function when MCLK divide by 1.5 is selected and VD = 3.3 V. When in Control Port mode, the following startup sequence will correct the problem.
  - Power up the part.
  - Hold MCLK Static
  - Hard reset vthe part
  - Set PDN
  - Set Reg. 00h value to 99h
  - Set Reg. 2Eh value to 89h
  - Finish initialization and start clocks
  - Release PDN

  There is no solution to this problem when operating the part in Hardware mode.
- In slave, Control Port mode, if the MCLK, SCLK or LRCK are applied when not in PDN or if either speed mode, MCLK divide or sample rate are changed, the retimer will not function properly and THD+N performance may be degraded. For proper retimer operation, the user should set the MCLK divide, then stabilize all clocks (while PDN is asserted) then release PDN. If the sample rate or speed mode changes with the part operational and out of PDN and the mclk/sclk timing relationship changes too, the user should power down the chip and power up again when in Control Port mode or apply a hard reset when in Hardware mode.