Errata: CS8422 Rev. B1 Silicon

(Reference CS8422_DS692PP1 Datasheet)

- The minimum TDM_IN setup time before OSCLK rising edge does not meet the data sheet specification. The minimum setup time is 14 ns for VL = 3.3 V and 5 V, and 18 ns for VL = 1.8 V and 2.5 V.

Contacting Cirrus Logic Support
For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to http://www.cirrus.com