WM8805_6152_DS28_EV1_REV3

Evaluation Board Example Configurations

INTRODUCTION

The WM8805 is a high performance S/PDIF transceiver which offers a state-of-the-art jitter attenuating S/PDIF receiver design.

The WM8805 customer evaluation board provides full functionality for the evaluation of the WM8805 device.

The purpose of this document is to detail common standard configurations for evaluation board operation. Contained in this document are:

- WM8805 internal signal path details.
- Register settings for internal configuration of the WM8805 device.
- Details on evaluation board setup and configuration.

This document can be used as a base line for evaluation board configuration when beginning to use the WM8805 customer evaluation board. Please note that all register settings supplied in this document are suitable to setup the required path but may not be optimised for quiet power up or other considerations that will be necessary for any end application. Please consult the latest datasheet for information on such considerations.

Software to configure the evaluation board can be downloaded from
http://www.wolfsonmicro.com/support/drivers

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TERMINOLOGY

AIF	Audio Interface
S/PDIF	Sony/Philips Digital Interface Format
USB	Universal Serial Bus
EVB	Evaluation Board
MCU	Microprocessor Control Unit

INPUTS AND OUTPUTS

BOARD POWER SUPPLIES

The WM8805 customer evaluation board can be powered using one of two sources:

- External power supplies
- Derived from the USB connection

The evaluation board can be powered either from the 4mm power lead receptacles or from the USB host. Refer to Table 1.

REF-DES	LINK STATUS	DESCRIPTION
J8 (PVDD_SEL)	1 - 2 2 - 3	**PVDD Power Source Select** PVDD 4mm power jack receptacle selected USB power source selected [default setting]
J9 (DVDD_SEL)	1 - 2 2 - 3	**DVDD Power Source Select** DVDD 4mm power jack receptacle selected USB power source selected [default setting]
J10 (DVDD_DAC_ SEL)	1 - 2 2 - 3	**S/PDIF Receiver DAC Power Source Select** DVDD 4mm power jack receptacle selected USB power source selected [default setting]
J11 (+5V_SEL)	1 - 2 2 - 3	**+5V Power Source Select** +5V 4mm power jack receptacle selected USB power source selected [default setting]

Table 1 Power Supply Source Select

Using appropriate power leads with 4mm connectors, supplies can be connected as described in Table 2 if the power supply is selected as the 4mm power jack receptacles.

REF-DES	SOCKET NAME	SUPPLY
J1	PVDD	+2.7V to +3.6V
J2	PGND	0V
J3	DVDD	+2.7V to +3.6V
J4	DGND	0V
J5	+5V	+5V

Table 2 Power Supply Connections

Note: Refer to the datasheet for limitations on individual supply voltages.

Important: Exceeding the recommended maximum voltage can damage EVB components. Under voltage may cause improper operation of some or all of the EVB components.

S/PDIF INPUTS

The WM8805 evaluation board supports both electrical and optical input of the S/PDIF stream. This signal may be input via a standard phono connector (J7 or J18) or via the optical receivers (U3 or U10). Refer to Table 3 for details.

REF-DES	CONNECTOR TYPE	DESCRIPTION
J7	Phono Connector	S/PDIF_IN_0_ELECTRICAL
J18	Phono Connector	S/PDIF_IN_1_ELECTRICAL
U3	Optical Receiver	S/PDIF_IN_0_OPTICAL
U10	Optical Receiver	S/PDIF_IN_1_OPTICAL

Table 3 S/PDIF Input Connections

The S/PDIF input stream must then be routed to the appropriate WM8805 pins using the optical/electrical input selection jumpers (J29 and J30) and the routing headers (H1 and H7). Refer to Table 4 for details.

REF-DES	LINK STATUS	DESCRIPTION
J29		**S/PDIF Input 0 Source Select**
	1 - 2	Optical input selected
	2 - 3	Electrical input selected [default setting]
J30		**S/PDIF Input 1 Source Select**
	1 - 2	Optical input selected
	2 - 3	Electrical input selected [default setting]
H1		**S/PDIF Input 0 Routing**
	1 - 2	Route input 0 to WM8805 Rx0 input [default setting]
	5 - 6	Route input 0 to WM8805 Rx4 input
	9 - 10	Route input 0 to WM8805 Rx2 input
	13 - 14	Route input 0 to WM8805 Rx6 input
H7		**S/PDIF Input 1 Routing**
	1 - 2	Route input 1 to WM8805 Rx1 input [default setting]
	5 - 6	Route input 1 to WM8805 Rx5 input
	9 - 10	Route input 1 to WM8805 Rx3 input
	13 - 14	Route input 1 to WM8805 Rx7 input

Table 4 S/PDIF Input and Routing Selection

S/PDIF OUTPUT

The WM8805 S/PDIF output can be output from the WM8805 evaluation board via a standard phono connector (J17). Refer to Table 5.

REF-DES	SOCKET TYPE	SIGNAL
J21	Phono Connector	S/PDIF_OUT

Table 5 S/PDIF Output Connections

The evaluation board is also equipped with a Wolfson WM8726 received audio demonstration DAC. Refer to “S/PDIF Receiver Audio Demonstration DAC” section.

WM8805 BASIC CONFIGURATION

The following jumpers are provided to allow easy configuration of the WM8805 in both hardware and software mode. It is important that the jumpers are correctly configured for the desired WM8805 function.

JUMPERS	JUMPER STATUS	DESCRIPTION		
		Hardware Mode (selected by J15)	**Software Mode (selected by J15)**	
J12	1 – 2 2 – 3	**Audio Interface Master/Slave Select** Select master mode Select slave mode	**No function – remove link**	
J13	1 – 2 2 – 3	**Audio Interface Configuration 1** High Low	**Control Interface Mode Select** Select 3-wire (SPI compatible) mode Select 2-wire (I2C compatible) mode	
J15	1 – 2 2 – 3	**Hardware/Software Mode Select** Software mode Hardware mode	**Hardware/Software Mode Select** Software mode Hardware mode	
J16	1 – 2 2 – 3	**Audio Interface Configuration 0** High Low	**No function – remove link**	
J17	1 – 2 2 – 3	**S/PDIF Transmitter Source Select** Audio interface received data S/PDIF received data	**2 Wire/I2C Mode** **Device Address** 0x76 0x74	**3 Wire/SPI Mode** **No function – remove link**

Table 6 Jumpers

MCU CONTROL (VIA USB)

The WM8805 evaluation board is equipped with a USB interface MCU which allows interconnection with a PC in conjunction with the WM8805-EV1S evaluation software. To enable software control via the USB MCU, the pins in header H2 must be interconnected as shown in Table 7. The links must be removed as shown in hardware and 2-Wire/I2C mode.

REF-DES	LINK STATUS	DESCRIPTION		
H2		**WM8005 to Control Interface MCU Connection**		
	1 – 2	**3-Wire/SPI Mode** Connect WM8805 CSB to USB MCU	**2-Wire/I2C Mode** Do Not Fit Link	**Hardware Mode** Do Not Fit Link
	3 – 4	Connect WM8805 SCLK to USB MCU	Connect WM8805 SCLK to USB MCU	Do Not Fit Link
	5 – 6	Connect WM8805 SDIN to USB MCU	Connect WM8805 SDIN to USB MCU	Do Not Fit Link
	7 – 8	Connect WM8805 SDOUT to USB MCU	Do Not Fit Link	Do Not Fit Link

Table 7 USB MCU Connections

LED INDICATORS

The WM8805 evaluation board has a number of LEDs. Their function is described in Table 8 LED Descriptions.

LINK STATUS (IF APPLICABLE)	LED	HARDWARE MODE DESCRIPTION		SOFTWARE MODE DESCRIPTION (DEFAULT SETTINGS)	
		LED OFF	LED ON	LED OFF	LED ON
Not applicable	LED1	USB firmware issue.	USB firmware OK.	USB firmware issue..	USB firmware OK.
Not applicable	LED2	USB power not present.	USB interface power is OK.	USB not present.	USB interface power is OK.
H4, 1 – 2 fitted (remove in s/w mode)	LED3	S/PDIF Rx TRANS_ERR status. Indicates that the S/PDIF RX has **not** received a transmission error.	S/PDIF Rx TRANS_ERR status. Indicates that the S/PDIF RX **has** received a transmission error.	Not applicable – do not fit link.	Not applicable– do not fit link.
H4, 3 – 4 fitted	LED4	No General Error occurred	GEN_FLAG – indicates a general error has occurred (logical OR of TRANS_ERR, NON_AUDIO and UNLOCK)	GPO0 – defaults to INT_N Indicates an interrupt **has** occurred due to change in S/PDIF Rx status	GPO0 – defaults to INT_N Indicates **no** interrupt due to change in S/PDIF Rx status
H4, 5 – 6 fitted	LED5	S/PDIF Rx UNLOCK status indicating that the S/PDIF RX has locked.	S/PDIF Rx UNLOCK status. Indicates that the S/PDIF RX has **lost lock.**	GPO1 – defaults to S/PDIF Rx UNLOCK status indicating that the S/PDIF RX has locked.	GPO1 – defaults to S/PDIF Rx UNLOCK status. Indicates that the S/PDIF RX has **lost** lock.
H4, 7 – 8 fitted (remove in 3-wire s/w mode)	LED6	S/PDIF Rx UNLOCK status indicating that the S/PDIF RX has **locked**.	S/PDIF Rx UNLOCK status. Indicates that the S/PDIF RX has **lost lock.**	**2-wire mode** GPO2– defaults to S/PDIF Rx UNLOCK status. Indicates that the S/PDIF RX has **locked**. **3-wire mode** NOT Available – remove link	**2-wire mode** GPO2– defaults to S/PDIF Rx UNLOCK status. Indicates that the S/PDIF RX has **lost lock.** **3-wire mode** NOT Available – remove link
H4, 9 – 10 fitted only if used as GPO3	LED7	NOT Available – remove link	NOT Available – remove link	GPO3 – defaults to S/PDIF Rx SFRM_CLK status indicating that the SFRM_CLK is LOW	GPO3 – defaults to S/PDIF Rx SFRM_CLK status indicating that the SFRM_CLK is HIGH
H4, 11 – 12 fitted only if used as GPO4	LED8	NOT Available – remove link	NOT Available – remove link	GPO4 – defaults to S/PDIF Rx 192BCLK status indicating that the 192BCLK is LOW	GPO4 – defaults to S/PDIF Rx 192BCLK status indicating that the 192BCLK is HIGH
H4, 13 – 14 fitted only if used as GPO5	LED9	NOT Available – remove link	NOT Available – remove link	GPO5 – defaults to S/PDIF Rx C bit status indicating that the 'C' bit is LOW	GPO5 – defaults to S/PDIF Rx C bit status indicating that the 'C' bit is HIGH
H4, 15 – 16 fitted only if used as GPO6	LED10	NOT Available – remove link	NOT Available – remove link	GPO6 – defaults to S/PDIF Rx U bit status indicating that the 'U' bit is LOW	GPO6 – defaults to S/PDIF Rx U bit status indicating that the 'U' bit is HIGH

LINK STATUS (IF APPLICABLE)	LED	HARDWARE MODE DESCRIPTION		SOFTWARE MODE DESCRIPTION (DEFAULT SETTINGS)	
		LED OFF	LED ON	LED OFF	LED ON
H4, 17 – 18. (remove in 3-wire s/w mode)	LED11	TRANS_ERR status. Indicates that the S/PDIF RX has **not** received a transmission error.	TRANS_ERR status. Indicates that the S/PDIF RX has received a transmission error.	**2-wire mode** GPO7– defaults to S/PDIF Rx TRANS_ERR status. Indicates that the S/PDIF RX has **not** received a transmission error. **3-wire mode** NOT Available – remove link	**2-wire mode** GPO7– defaults to S/PDIF Rx TRANS_ERR status. Indicates that the S/PDIF RX has received a transmission error. **3-wire mode** NOT Available – remove link

Table 8 LED Descriptions

EXAMPLE CONFIGURATIONS

The following example configurations are independent of whether power is applied to the board from external power supplies or from the USB interface.

HARDWARE MODE EXAMPLES

In hardware control mode the WM8805 can only receive data from S/PDIF RX0.

S/PDIF RECEIVER RX0 TO AIF

The configuration is as follows:-

- Data path = S/PDIF RX0 (electrical input) to AIF DOUT
- Hardware master mode.
- Powered from the USB interface.
- AIF format = 24 bit I^2S
- Figure 1 illustrates the data path.
- Figure 2 illustrates the jumpers which must be made on the board.

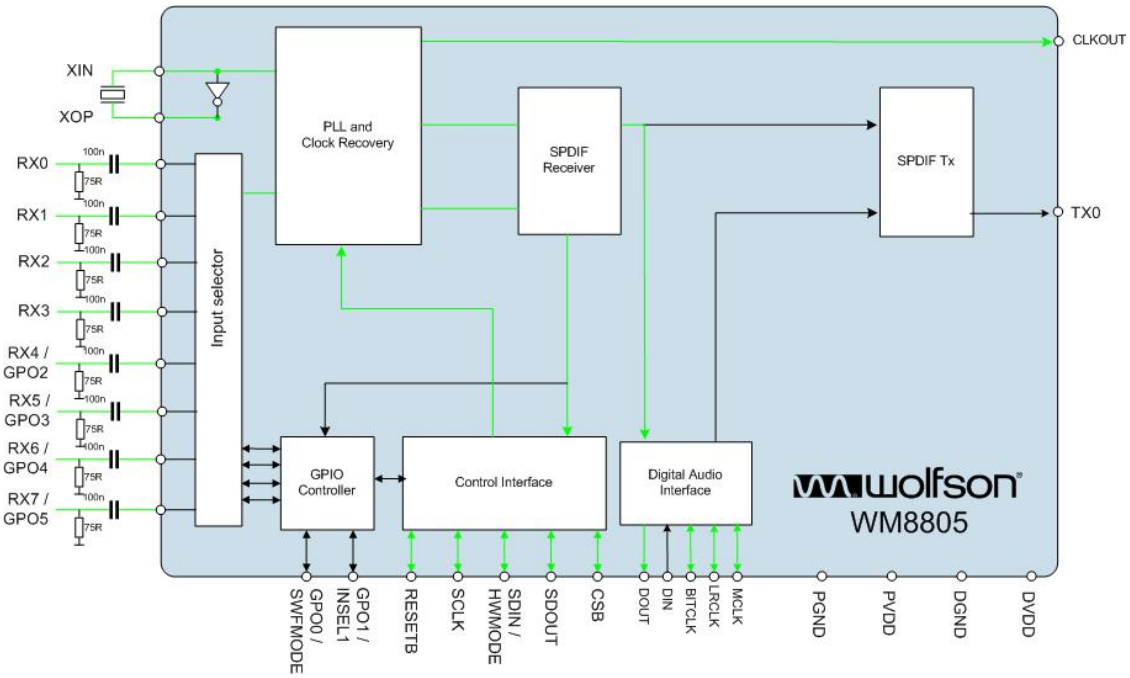

Figure 1 RX0 Input Path to Audio Interface Block Diagram

To configure this path, with an audio interface format of 24 bit I^2S, the external jumpers should be set as shown in Table 9. Do not fit H2 links.

JUMPERS	JUMPER STATUS	DESCRIPTION
J12	1 – 2	**Audio Interface Master/Slave Select** Select master mode
J16	1 – 2	**Audio Interface Configuration 0** High
J13	2 – 3	**Audio Interface Configuration 1** Low
J15	2 – 3	**Hardware/Software Mode Select** Hardware mode
J17	1 – 2	**S/PDIF Transmitter Source Select** Audio interface received data
J29	1 – 2	**S/PDIF Input 0 Source Select** Electrical input selected
H1	1 – 2	**S/PDIF Input 0 Routing** Route input 0 to WM8805 Rx0 input

Table 9 RX0 Input Path to Audio Interface Link Settings

The jumpers, input signals and output signals are shown in Figure 2. The yellow jumpers are those that are required. The red jumpers are for power.

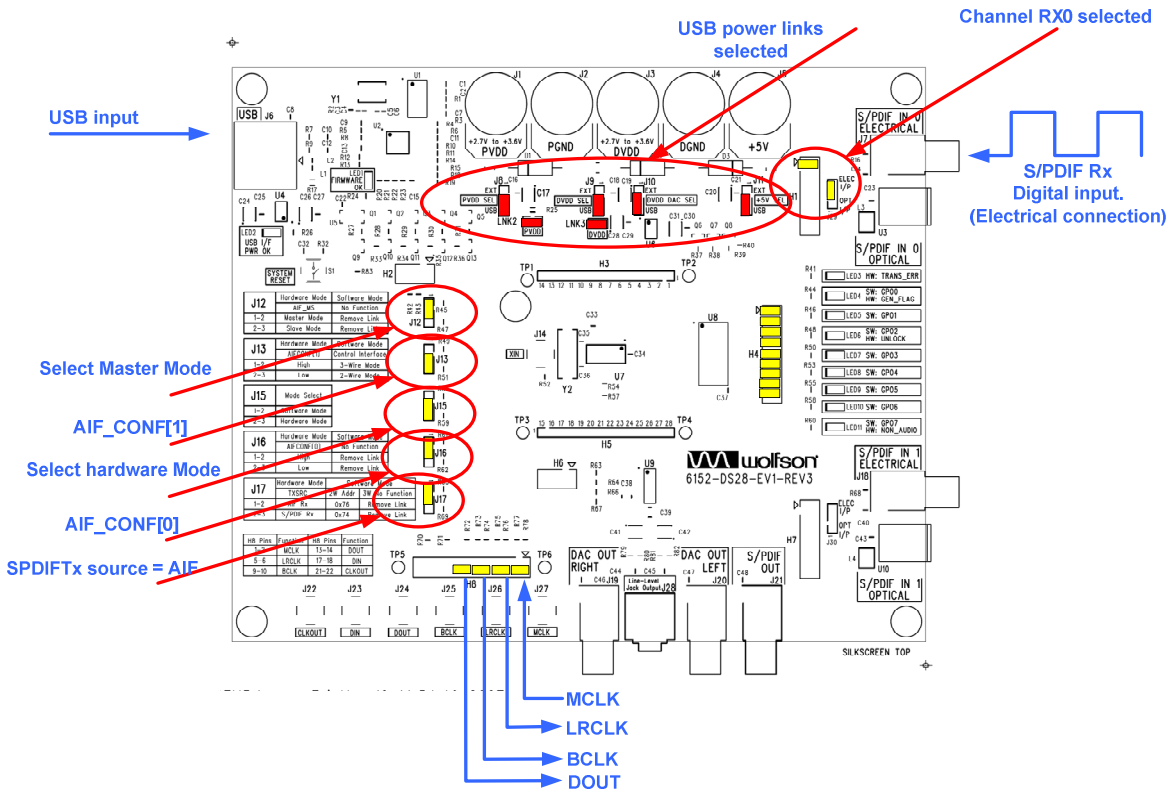

Figure 2 RX0 Input Path to Audio Interface Evaluation Board Configuration

Data is applied to the S/PDIF RX0 interface. The output data can be monitored at the AIF DOUT. MCLK is an output from the AIF.

S/PDIF RECEIVER RX0 TO S/PDIF TRANSMITTER

The configuration is as follows:-

- Data path = S/PDIF RX0 (optical input) to S/PDIF TX
- Hardware slave mode.
- Powered from the USB interface.
- AIF format = 24 bit I^2S
- Figure 3 illustrates the data path.
- Figure 4 illustrates the jumpers which must be made on the board.

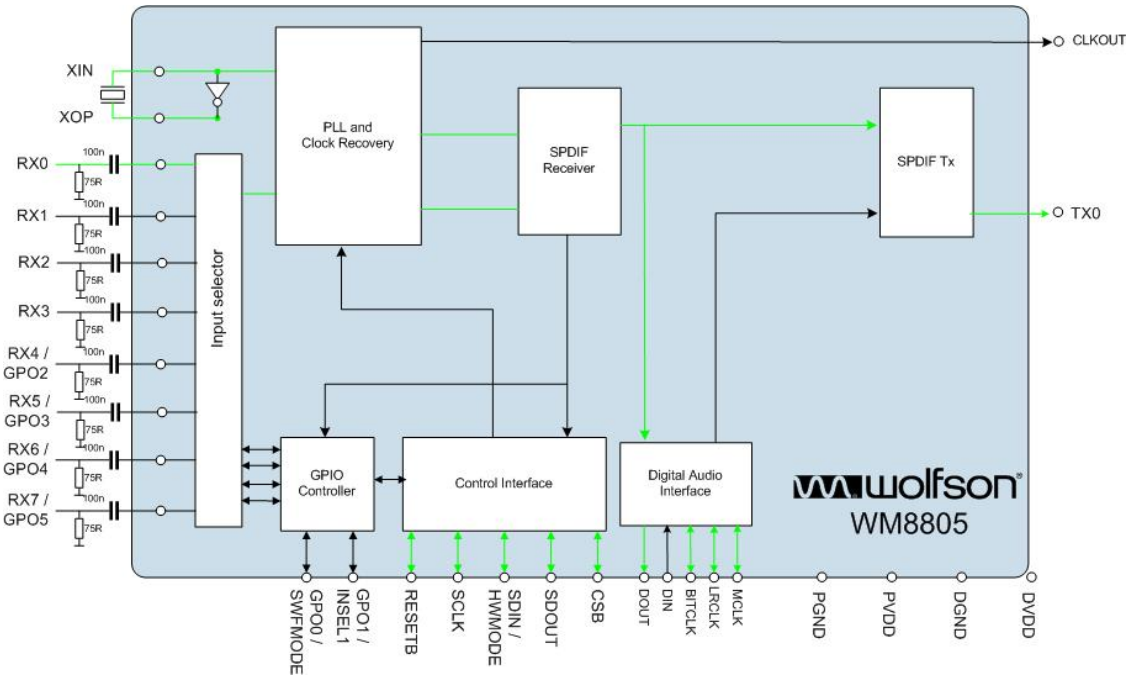

Figure 3 S/PDIF RX0 Input to S/PDIFTX0 Output Block Diagram

To configure this path, with an audio interface format of 24 bit I^2S, the external jumpers should be set as shown inTable 10. Do not fit H2 links.

JUMPERS	JUMPER STATUS	DESCRIPTION
J12	2 – 3	**Audio Interface Master/Slave Select** Select slave mode
J16	1 – 2	**Audio Interface Configuration 0** High
J13	2 – 3	**Audio Interface Configuration 1** Low
J15	2 – 3	**Hardware/Software Mode Select** Hardware mode
J17	2 – 3	**S/PDIF Transmitter Source Select** S/PDIF received data
J29	2 – 3	**S/PDIF Input 0 Source Select** Optical input selected
H1	1 – 2	**S/PDIF Input 0 Routing** Route input 0 to WM8805 Rx0 input

Table 10 S/PDIF RX0 Input Path to S/PDIF TX Link Settings

The jumpers, input signals and output signals are shown in Figure 4. The yellow jumpers are those that are required.

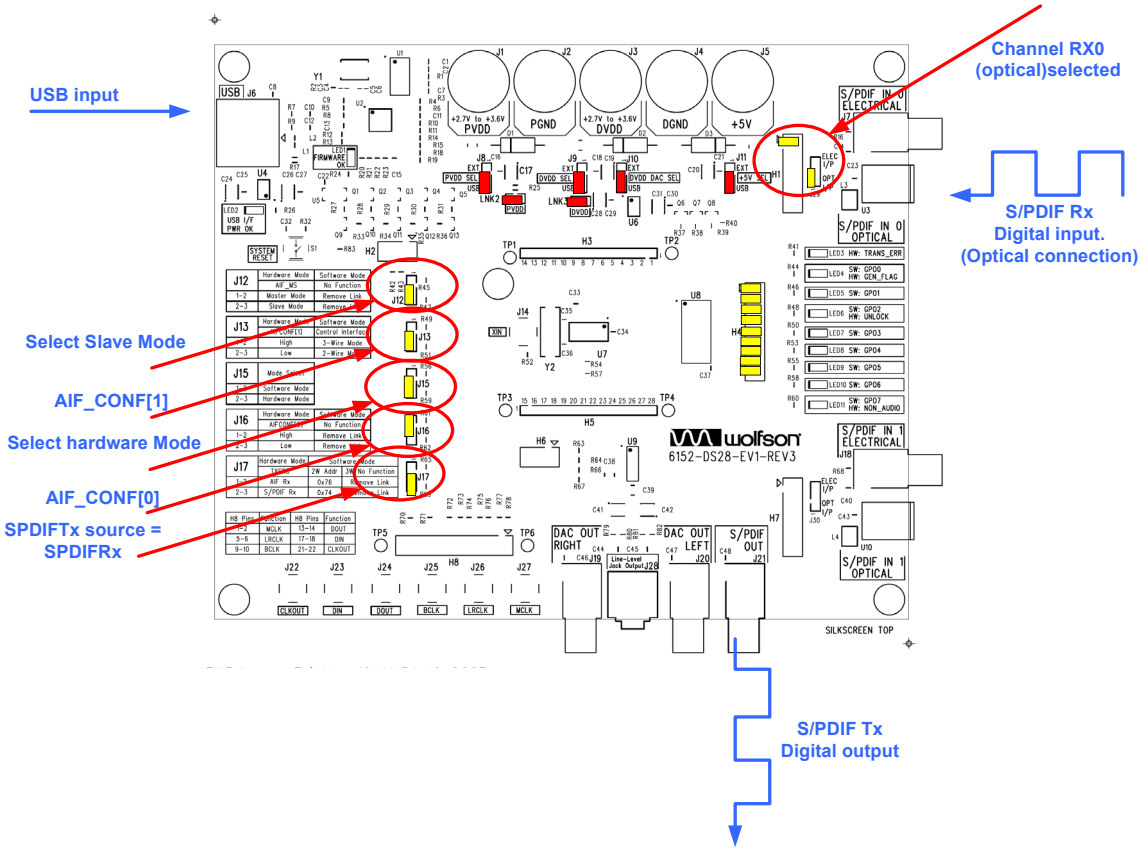

Figure 4 S/PDIF RX0 (optical) Input Path to S/PDIF TX Output Evaluation Board Configuration

AIF TO S/PDIF TRANSMITTER

The configuration is as follows :-

- Data path = AIF to S/PDIF TX
- Hardware slave mode.
- Powered from the USB interface.
- AIF format = 24 bit I^2S
- Figure 5 illustrates the data path.
- Figure 6 illustrates the jumpers which must be made on the board.

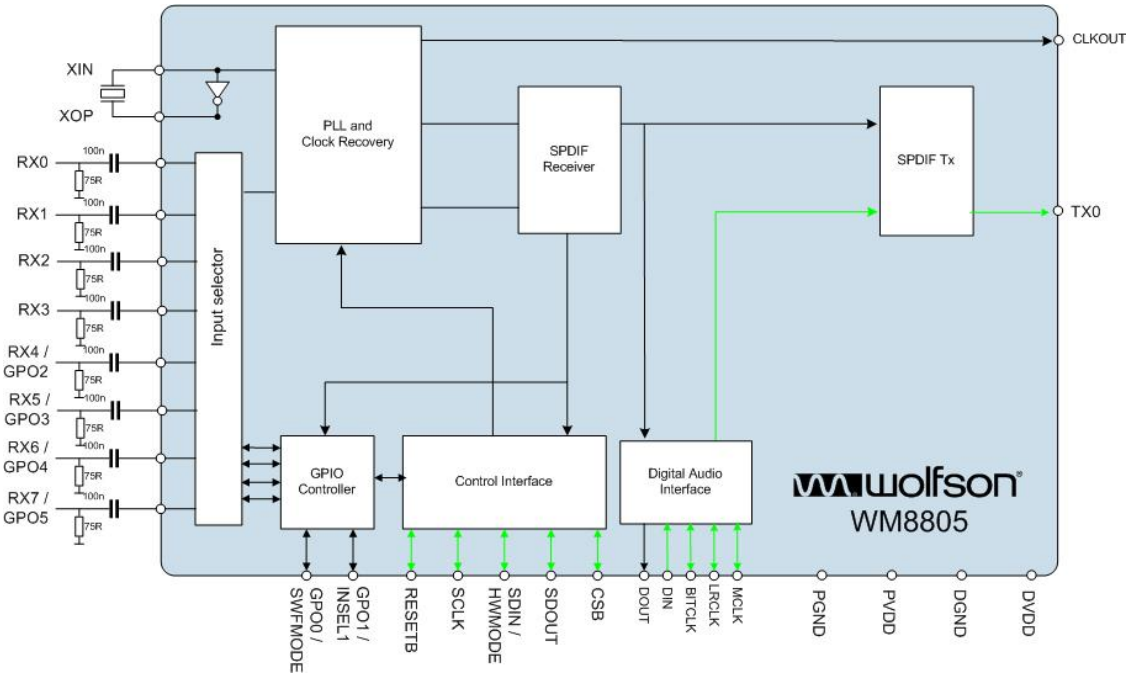

Figure 5 Audio Interface to TX0 Block Diagram

To configure this path, with an audio interface format of 24 bit I^2S, the external jumpers should be set as shown in Table 11. Do not fit H2 links.

JUMPERS	JUMPER STATUS	DESCRIPTION
J12	2 – 3	**Audio Interface Master/Slave Select** Select slave mode
J16	1 – 2	**Audio Interface Configuration 0** High
J13	2 – 3	**Audio Interface Configuration 1** Low
J15	2 – 3	**Hardware/Software Mode Select** Hardware mode
J17	1 – 2	**S/PDIF Transmitter Source Select** Audio interface received data

Table 11 AIF Input Path to S/PDIF TX Link Settings

The jumpers, input signals and output signals are shown in Figure 6. The yellow jumpers are those that are required.

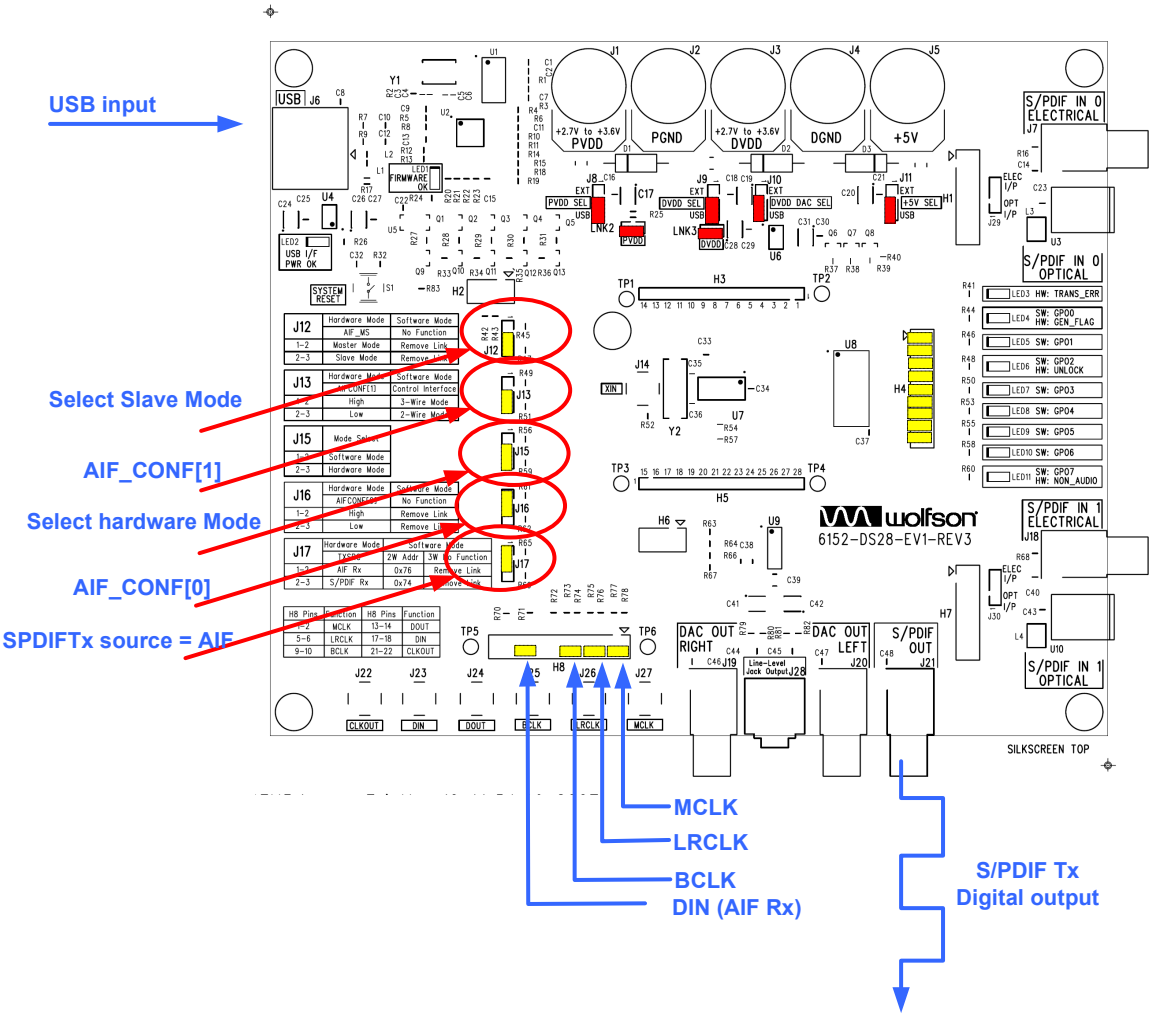

Figure 6 AIF Input Path to S/PDIF TX Output Evaluation Board Configuration

SOFTWARE MODE EXAMPLES

S/PDIF RECEIVER RX1 TO AIF

The configuration is as follows:-

- Data path = S/PDIF RX1 (electrical input) to AIF DOUT
- Software slave mode. 3-wire control interface
- Powered from the USB interface.
- AIF format = 24 bit I^2S
- Figure 7 illustrates the data path.
- Figure 8 illustrates the jumpers which must be made on the board.

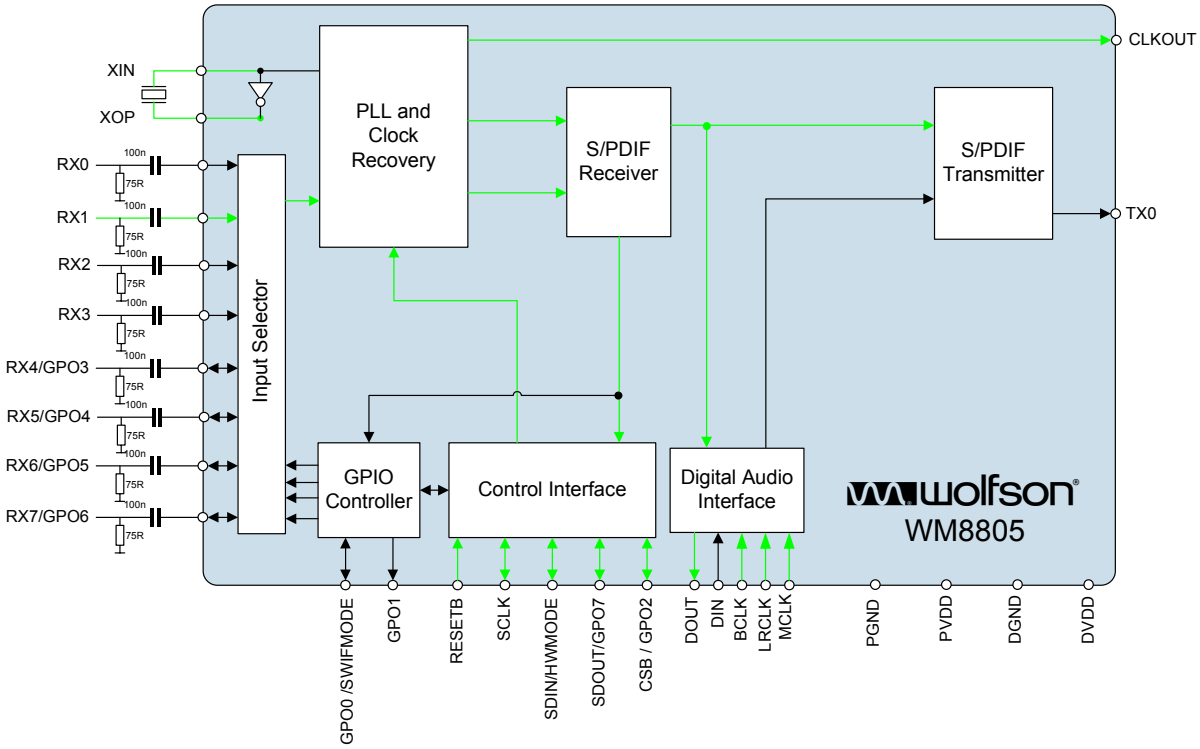

Figure 7 S/PDIF Rx1 to Audio Interface Block Diagram

To configure this path, with an audio interface format of 24 bit I^2S, the external jumpers should be set as shown in Table 12 and the registers programmed as in Table 13

JUMPERS	JUMPER STATUS	DESCRIPTION
J13	1 – 2	**Control Interface Mode Select** Select 3-wire (SPI compatible) mode
J15	1 – 2	**Hardware/Software Mode Select** Software mode

Table 12 Jumper Settings for S/PDIF Rx1 to Audio Interface

REGISTER	SETTING	COMMENT
0x00	0x00	Reset device
0x1E	0x04	Disable the S/PDIF Tx interface
0x08	0x01	Select S/PDIF Rx1 channel input
0x09	0x02	Select the comparator input mode for Rx1
0x1B	0x0A	AIF Tx = 24 bit, I^2S
0x1C	0x0A	Slave mode, AIF Rx = 24 bit, I^2S

Table 13 Register Settings for S/PDIF Rx1 to Audio Interface

The jumpers, input signals and output signals are shown in Table 8. The yellow jumpers are those that are required.

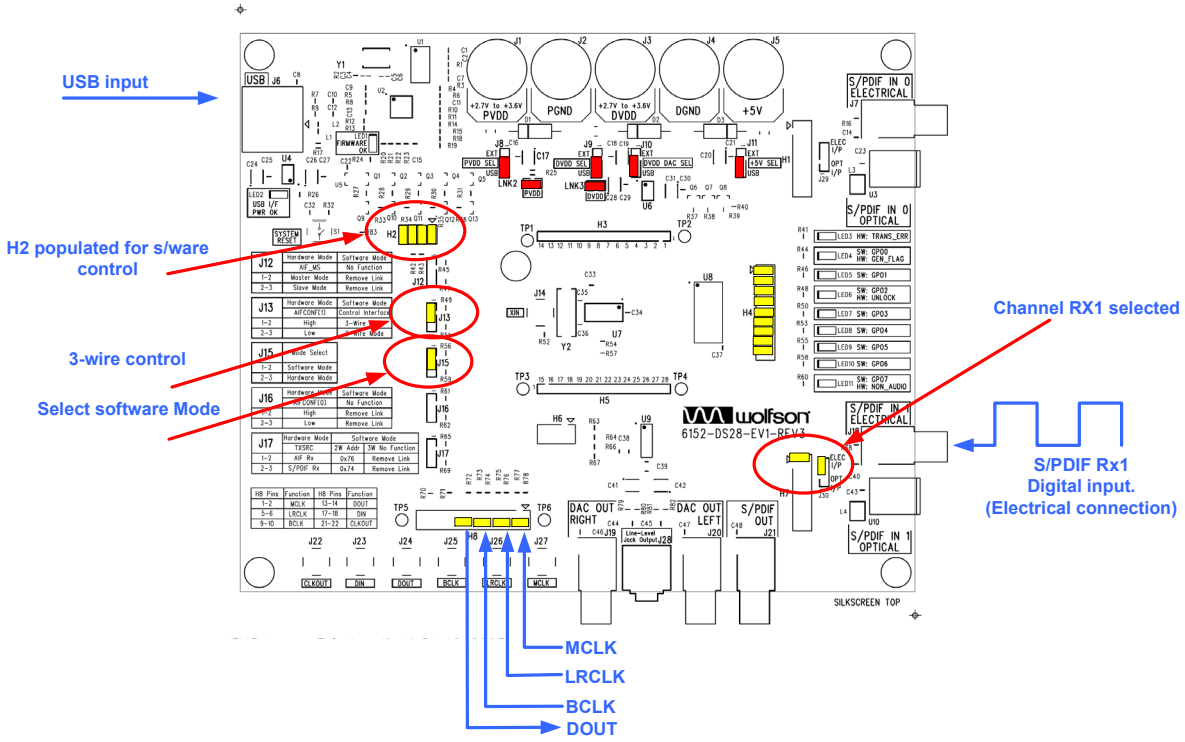

Figure 8 RX1 Input Path to Audio Interface Evaluation Board Configuration

S/PDIF RECEIVER RX4 TO S/PDIF TRANSMITTER

The configuration is as follows:-

- Data path = S/PDIF RX4 (electrical input) CMOS compatible to S/PDIF Tx
- Software Mater mode. 2-wire control interface. Address=0x76.
- Powered from external power supplies.
- AIF format = 24 bit I^2S
- Figure 9 illustrates the data path.
- Figure 10 illustrates the jumpers which must be made on the board.

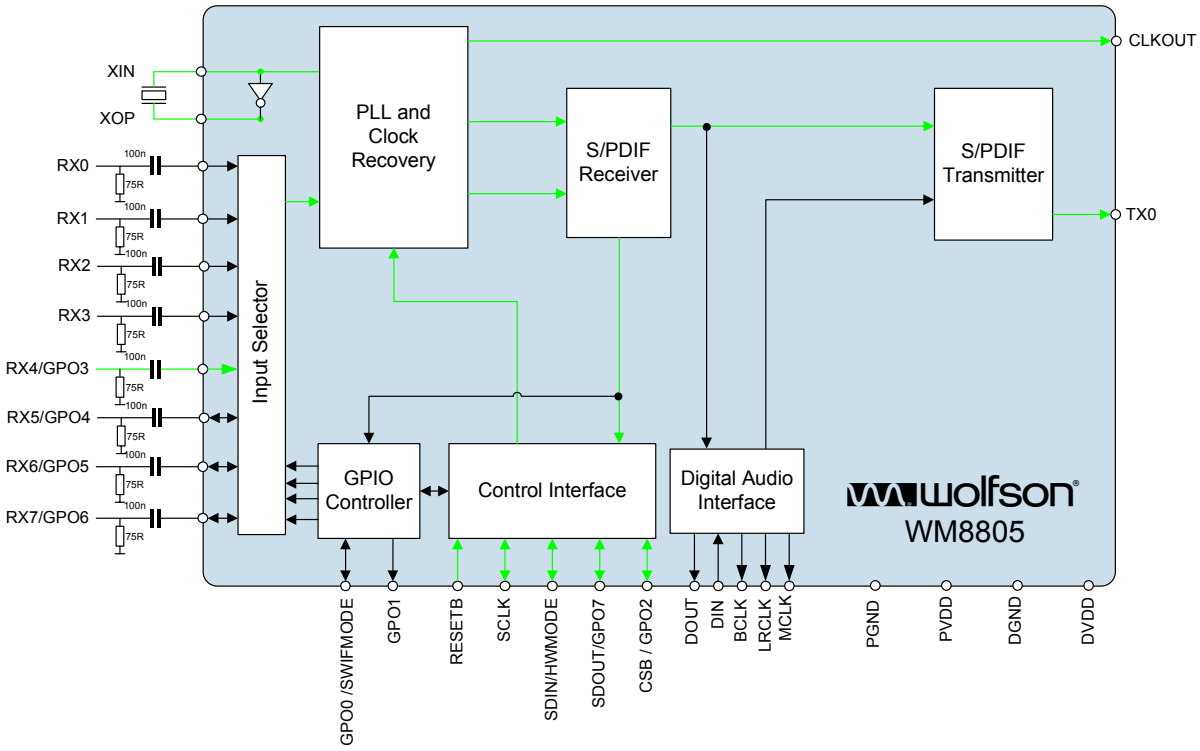

Figure 9 Rx4 to TX0 Block Diagram

To configure this path, with an audio interface format of 24 bit I^2S, the external jumpers should be set as shown in Table 14 and the registers programmed as in Table 15.

JUMPERS	JUMPER STATUS	DESCRIPTION
J13	2 – 3	**Control Interface Mode Select** Select 2-wire (I2C compatible) mode
J15	1 – 2	**Hardware/Software Mode Select** Software mode
J17	1 – 2	**2 Wire/I2C Mode** **Device Address** 0x76

Table 14 Jumper Settings for S/PDIF Rx4 to S/PDIF Tx

REGISTER	SETTING	COMMENT
0x00	0x00	Reset device
0x1E	0x10	Disable the AIF
0x08	0x04	Select S/PDIF Rx4 channel input
0x09	0x00	Select the CMOS compatible input mode for Rx4
0x15	0x31	S/PDIF Tx source= S/PDIF Rx
0x1B	0x0A	AIF Tx = 24 bit, I^2S
0x1C	0x4A	Master mode, AIF Rx = 24 bit, I^2S

Table 15 Register Settings for S/PDIF Rx4 to S/PDIF Tx

The jumpers, input signals and output signals are shown in Figure 10. The yellow jumpers are those that are required.

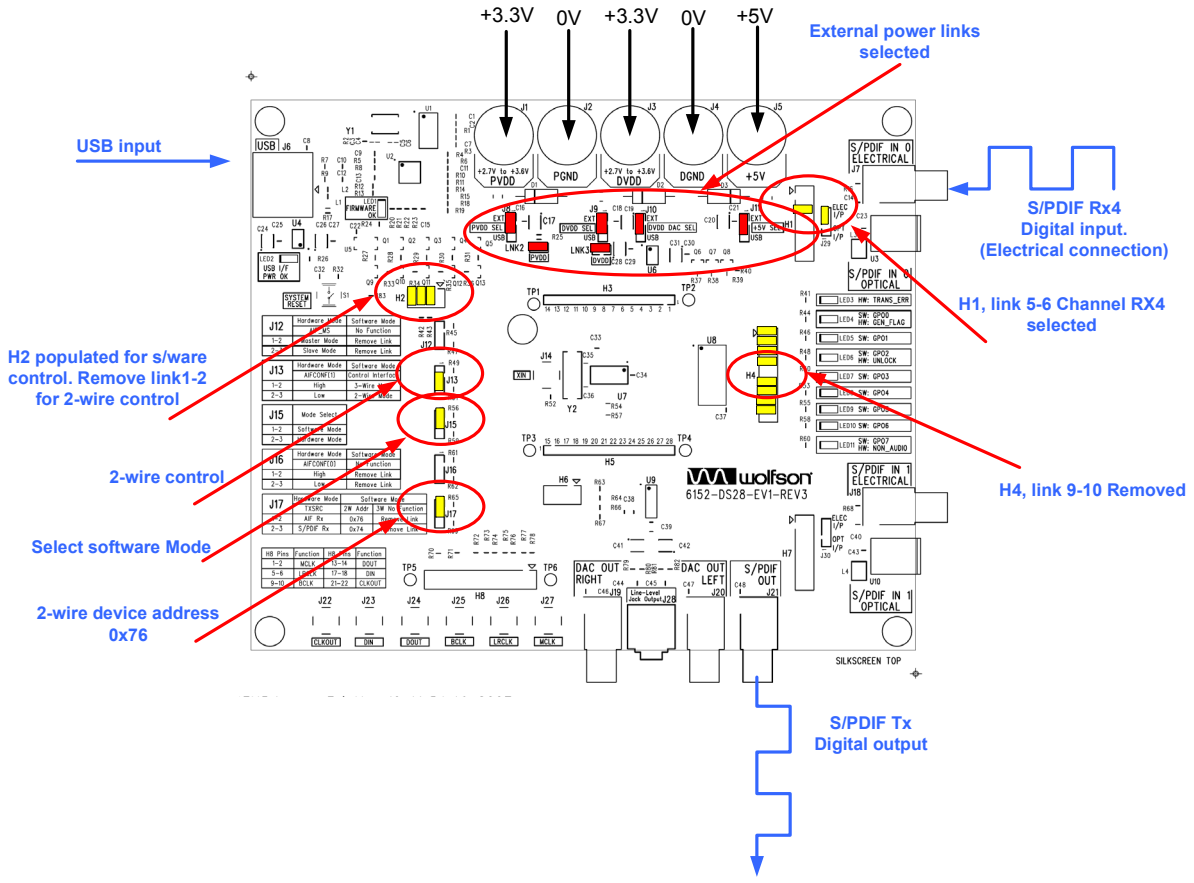

Figure 10 S/PDIF RX4 Input to S/PDIF Tx Configuration

S/PDIF RECEIVER AUDIO DEMONSTRATION DAC

The following configuration illustrates the S/PDIF Rx to analogue output via the WM8726 DAC. This can be used to view an analogue representation of the digital data received on the selected S/PDIF Rx interface. Note that the AIF should not be connected to any other test equipment if using this output.

This example also illustrates the connections needed when using an external power source instead of powering the board from the USB interface.

The configuration is as follows:-

- Data path = S/PDIF Rx2 to AIF
- Software Mater mode. 2-wire control interface. Address=0x74.
- Powered from external power supplies.
- AIF format = 24 bit I^2S

Figure 11 illustrates the jumpers which must be made on the board. The jumpers needed for external power supply are detailed in Table 1. Other external jumpers should be set as shown in Table 16 and the registers programmed as in Table 17.

JUMPERS	JUMPER STATUS	DESCRIPTION
J13	**2 – 3**	**CONTROL INTERFACE MODE SELECT** Select 2-wire (I2C compatible) mode
J15	**1 – 2**	**HARDWARE/SOFTWARE MODE SELECT** Software mode
J17	**2 – 3**	**2 WIRE/I2C MODE** Device Address =0x74

Table 16 Jumper Settings for S/PDIF Rx1 to Audio Interface

REGISTER	SETTING	COMMENT
0x00	0x00	Reset device
0x1E	0x04	Disable the S/PDIF Tx interface
0x08	0x02	Select S/PDIF Rx2 channel input
0x09	0x04	Select the comparator input mode for Rx2
0x1B	0x0A	AIF Tx = 24 bit, I^2S
0x1C	0x4A	Master mode, AIF Rx = 24 bit, I^2S

Table 17 Register Settings for S/PDIF Rx2 to Audio Interface

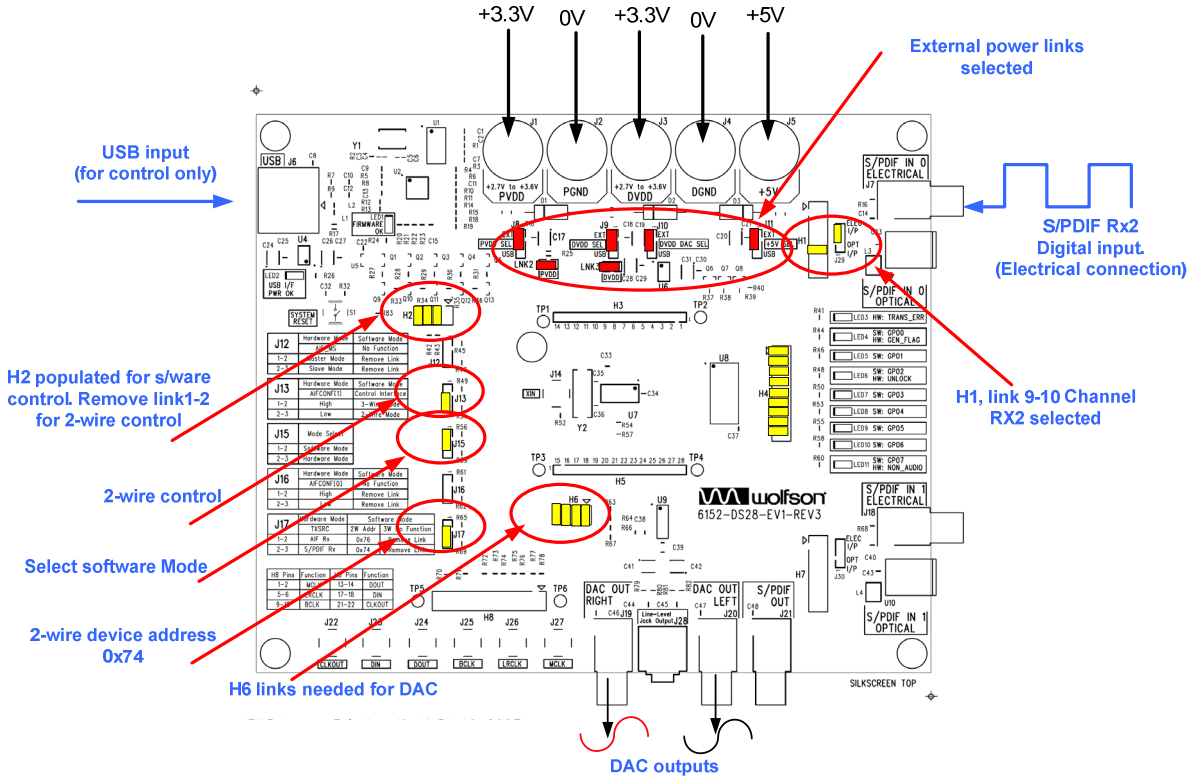

Figure 11 DAC Evaluation Board Configuration

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