WM8918-6201-FL32-M-REV1

Example Configurations

DOC TYPE:	EXAMPLE CONFIGURATIONS
BOARD REFERENCE:	WM8918-6201-FL32-M-REV1
BOARD TYPE:	Customer Mini Board
WOLFSON DEVICE(S):	WM8918
DATE:	July 2010
DOC REVISION:	Rev 1.0

INTRODUCTION

The WM8918-6201-FL32-M-REV1 Customer Mini Board is compatible with the 6201-EV1-REV3 customer evaluation board and together provide a complete hardware platform for evaluation of the WM8918. The WM8918 Customer Mini Board can also be used independently and connected directly to a processor board using flying wires or appropriate headers. This document will cover both, but performance data will be based on the Wolfson system with 6201-EV1-REV3 main board. Configurations covered are listed below:

- Electrical S/PDIF DAC to headphone playback
- Optical S/PDIF DAC to lineout playback
- Line-in bypass to headphone output
- USB streaming DAC to headphone playback

This document should be used as a starting point for evaluation of WM8918 but it will not cover every possible configuration.

Assumptions:

1. The user is familiar with the 6201-EV1-REV3 main board and that the board is correctly configured for the path of interest (see related documents below).
2. The user has control of the WM8918 register settings, for example by installing Wolfson WISCE software.

Related documents:

1. WM8918 datasheet
2. WM8918-6201-FL32-M-REV1 Schematic and Layout.pdf
3. 6201-EV1-REV3 Schematic and Layout.pdf
4. WISCE Quick Start Guide.pdf
5. Application Note WAN0240 – USB Audio Streaming

TABLE OF CONTENTS

BOARD CONFIGURATION STAND-ALONE

The WM8918 Customer Mini Board can be used as a stand-alone module for direct connection to a processor board via flying leads or dedicated headers. This section will detail important considerations and provide all information required to do this without risking damage to the device.

CONNECTION DIAGRAM

Figure 1 below shows the connections required to power-up and control the WM8918 Customer Mini Board.

Please refer to the Table 1 for further detail on external I/O connections.

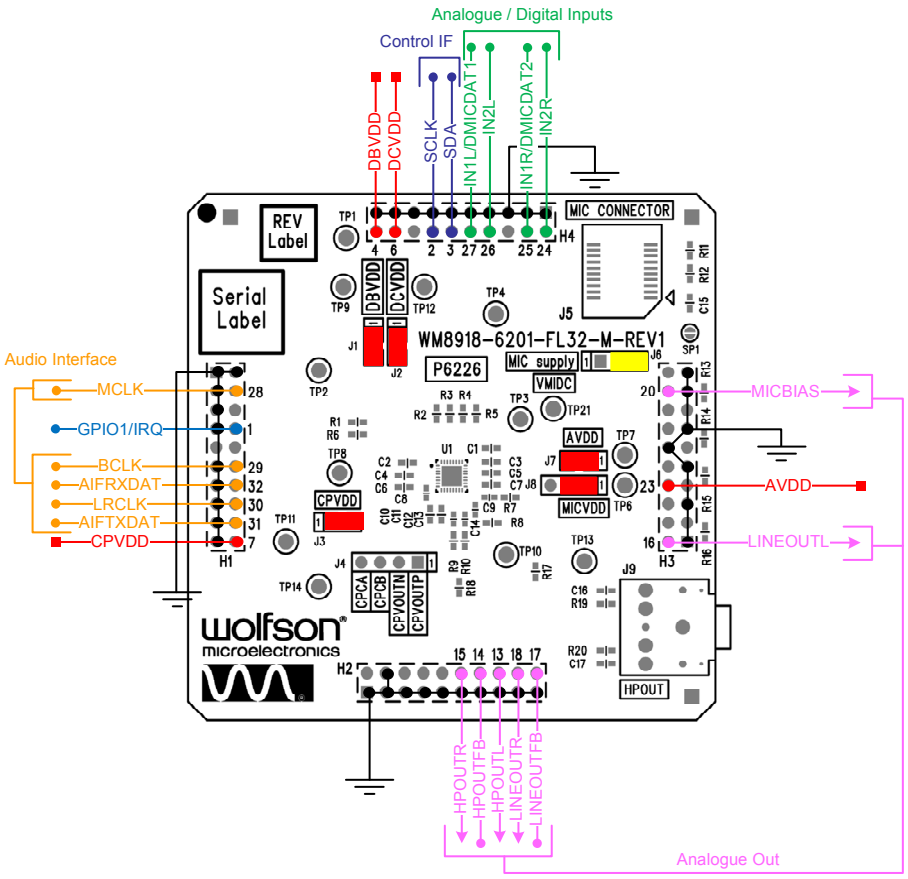


Figure 1 Stand-Alone Board Configuration

I/O TABLE

SIGNAL	BOARD REFERENCE	IMPORTANT NOTES
Voltage Supplies		
AVDD	H3: pin 8	AVDD = 1.71V to 2.0V
CPVDD	H1: pin 20	CPVDD = 1.71V to 2.0V
DCVDD	H4: pin 18	DCVDD = 0.95V to 1.98V
DBVDD	H4: pin 20	DBVDD = 1.42V to 3.6V
Ground		
DGND	Common Ground	Analogue and digital grounds must always be within 0.3V of each other.
AGND		
CPVDD		
Control Interface		
SDA	H4: pin 12	Both control interface signals should swing between DGND and DBVDD.
SCLK	H4: pin 14	
Master Clock		
MCLK	H1: pin 4	Signal should swing between DGND and DBVDD.
Digital I/O and Audio Interface		
GPIO1/IRQ	H1: pin 8	Signals should swing between DGND and DBVDD.
BCLK/GPIO4	H1: pin 12	
AIFRXDAT	H1: pin 14	
LRCLK	H1: pin 16	
AIFTXDAT	H1: pin 18	
Analogue Outputs		
HPOUTL	H2: pin 16	Ground referenced headphone output.
HPOUTR	H2: pin 12	
HPOUTFB	H2: pin 14	HP reference pin, recommended to be connected to the common ground at headphone connector.
LINEOUTL	H3: pin 2	Ground referenced line output.
LINEOUTR	H2: pin 18	
LINEOUTFB	H2: pin 20	LINE reference pin, recommended to be connected to the common ground at line output connector.
MICBIAS	H3: pin 18	Analogue microphone bias voltage output.
Analogue / Digital Inputs		
IN2R	H4: pin 2	Observe maximum input levels as per WM8918 datasheet.
IN1R/DMICDAT2	H4: pin 4	
IN2L	H4: pin 8	
IN1L/DMICDAT1	H4: pin 10	
Charge Pump and VMID		
CPVOUTP	J4: pin 1	Charge Pump and VMIDC test points.
CPVOUTN	J4: pin 2	
CPCA	J4: pin 4	
CPCB	J4: pin 3	
VMIDC	TP21	

Table 1 I/O Configuration

BOARD CONFIGURATION WITH 6201-EV1-REV3 MAIN BOARD

This section focuses on evaluation of the WM8918-6201-FL32-M-REV1 Customer Mini Board in combination with the 6201-EV1-REV3 main board. This system is the reference platform for measurement data contained in this document. Please note that only a limited number of usage modes will be covered.

ELECTRICAL S/PDIF DAC TO HEADPHONE PLAYBACK

The following section details board configuration for DAC to headphone playback using the S/PDIF electrical input.

BLOCK DIAGRAM

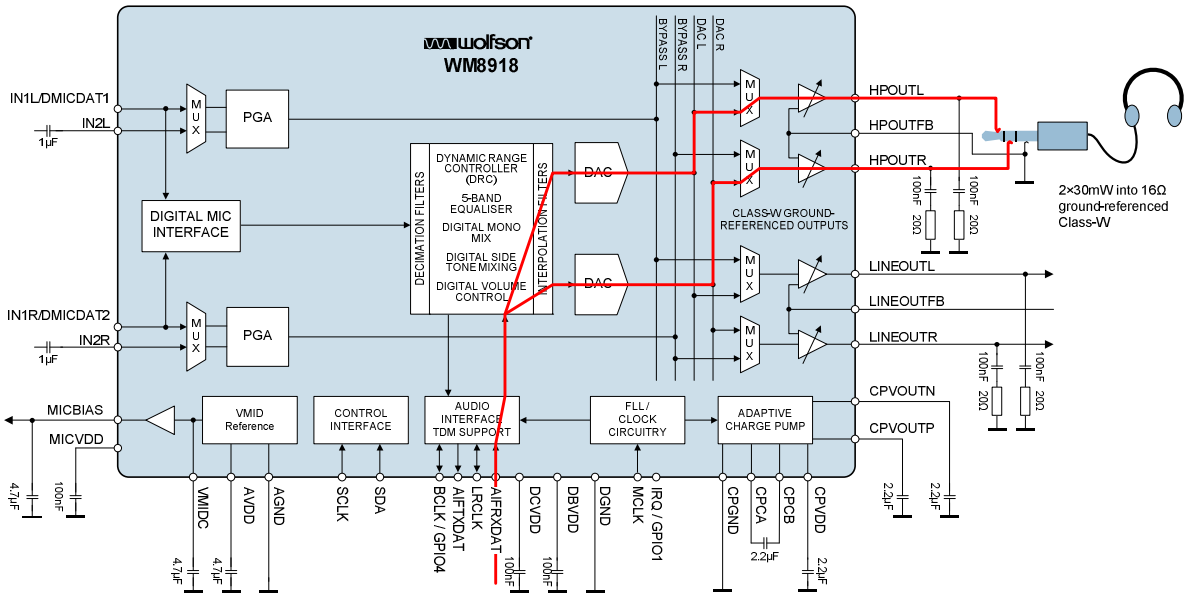


Figure 2 Path Diagram for DAC to Headphone Playback

BOARD CONFIGURATION

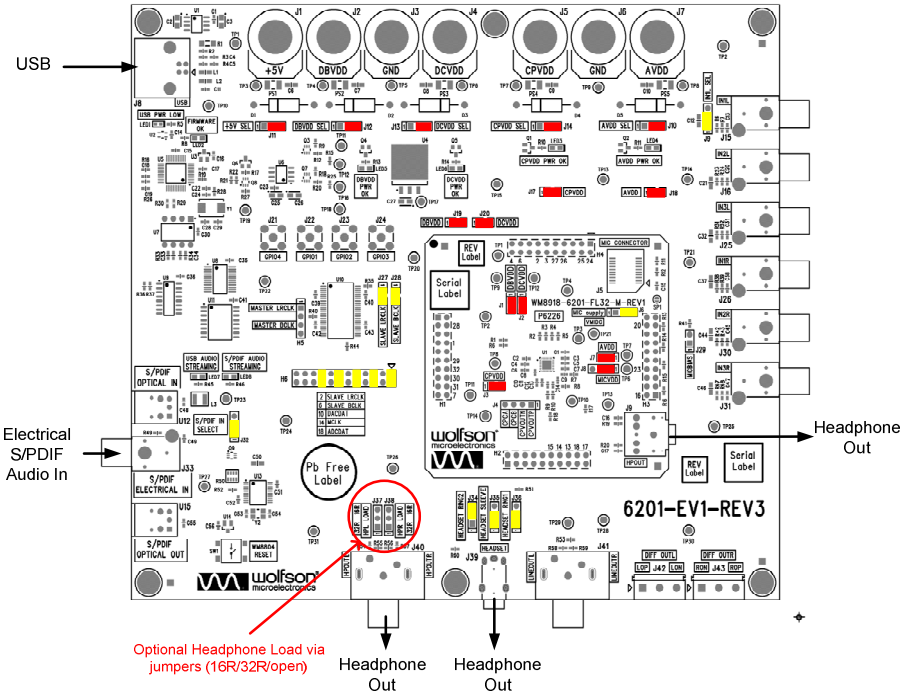


Figure 3 Board Configuration for Electrical S/PDIF DAC to Headphone

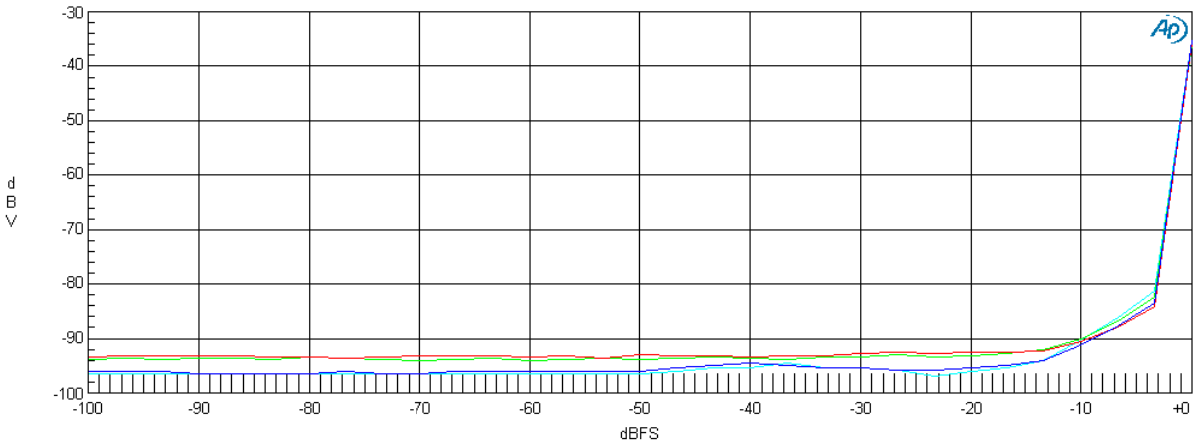
REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	Software Reset
0x16	0x0006	MCLK_INV=0, SYSCLK_SRC=0, MCLK_SRC=0, TOCLK_RATE=0, ADC_DIV=000, DAC_DIV=000, OPCLK_ENA=0, CLK_SYS_ENA=1, CLK_DSP_ENA=1, TOCLK_ENA=0
0x6C	0x0100	WSEQ_ENA=1, WSEQ_WRITE_INDEX=0_0000
0x6F	0x0100	WSEQ_ABORT=0, WSEQ_START=1, WSEQ_START_INDEX=00_0000
0x14	0x845E	TOCLK_RATE_DIV16=0, TOCLK_RATE_X4=0, SR_MODE=0, MCLK_DIV=0
0x39	0x0039	HPOUTL_MUTE=0, HPOUT_VU=0, HPOUTLZC=0, HPOUTL_VOL=11_1001
0x3A	0x00B9	HPOUTR_MUTE=0, HPOUT_VU=1, HPOUTRZC=0, HPOUTR_VOL=11_1001
0x21	0x0000	DAC_MONO=0, DAC_SB_FILT=0, DAC_MUTERATE=0, DAC_UNMUTE_RAMP=0, DAC_OSR128=0, DAC_MUTE=0, DEEMPH=00
0x68	0x0005	CP_DYN_PWR=1

Table 2 Register Settings for DAC to Headphone Playback

PERFORMANCE PLOT



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Anlr.THD+N Ampl	Left	22Hz-22kHz, A-Weighted, Left
1	2	Blue	Solid	1	Anlr.THD+N Ampl	Left	22Hz-22kHz, A-Weighted, Right
2	1	Green	Solid	1	Anlr.THD+N Ampl	Left	22Hz-20kHz, AES17, Left
2	2	Red	Solid	1	Anlr.THD+N Ampl	Left	22Hz-20kHz, AES17, Right

System: AP2
Board: 6201-EV1-REV3 + WM8918-6201-FL32-M-REV1
Manufacturer Mark Code: DWS
Input Path: Electrical S/PDIF In
Input Signal: 997Hz, 24-bit, 256fs
Output Path: HPOUT 32R
Supplies: AVDD=CPVDD=DBVDD=DCVDD=1V8
BW Filter: As stated in comments
Additional Filter: As stated in comments

Figure 4 Performance Plot for DAC to HPOUT with 32R Load

OPTICAL S/PDIF DAC TO LINEOUT PLAYBACK

The following section details board configuration for DAC to lineout playback using the S/PDIF optical input.

BLOCK DIAGRAM

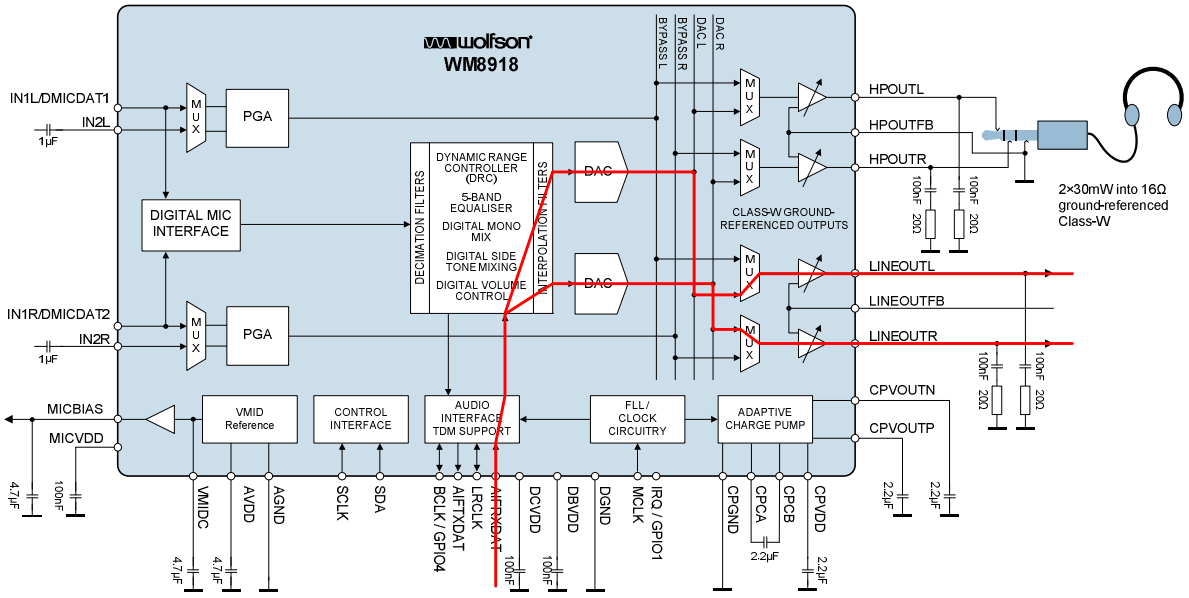


Figure 5 Path Diagram for DAC to Lineout Playback

BOARD CONFIGURATION

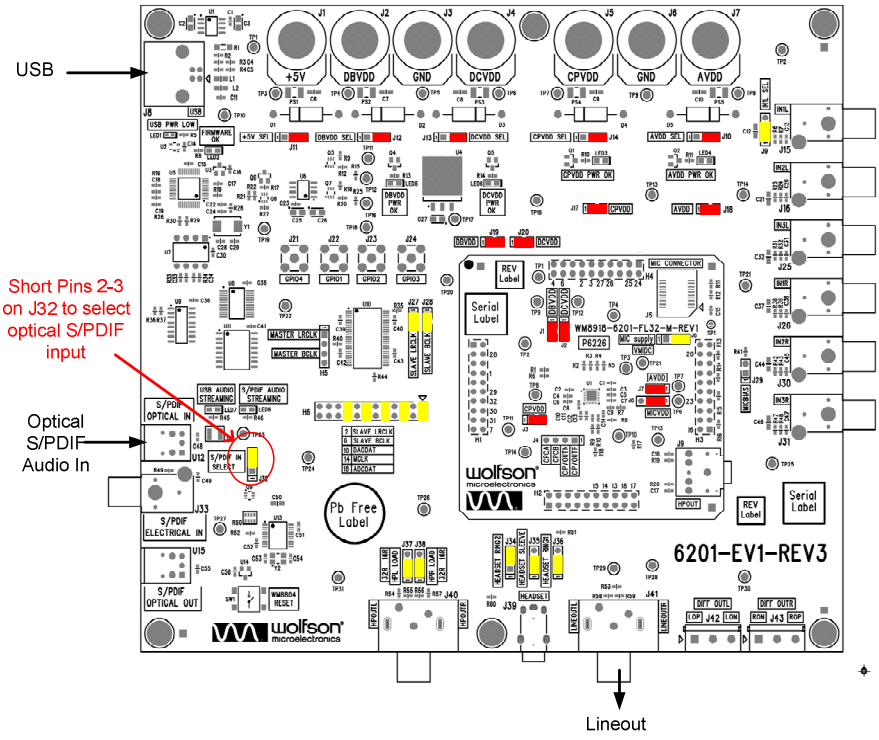


Figure 6 Board Configuration for Optical S/PDIF DAC to Lineout

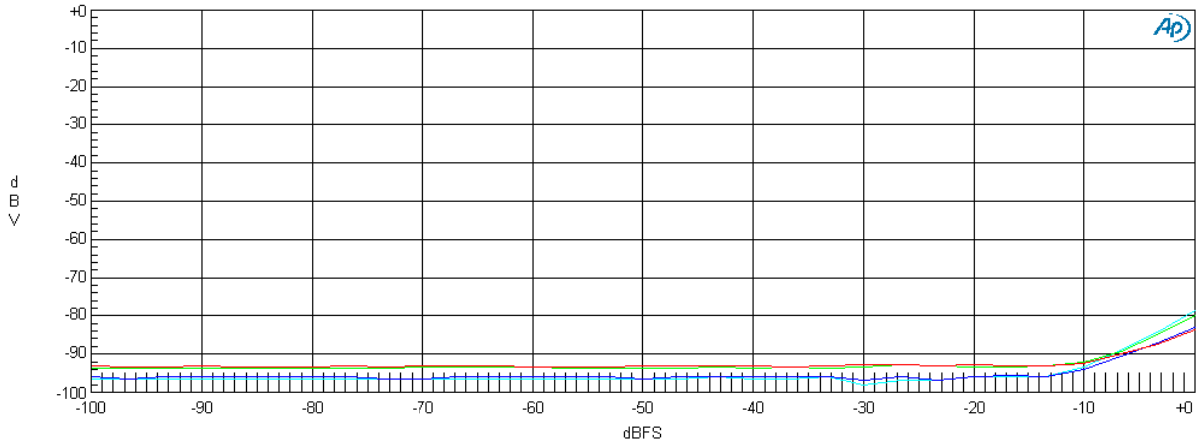
REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	Software Reset
0x16	0x0006	MCLK_INV=0, SYSCLK_SRC=0, MCLK_SRC=0, TOCLK_RATE=0, ADC_DIV=000, DAC_DIV=000, OPCLK_ENA=0, CLK_SYS_ENA=1, CLK_DSP_ENA=1, TOCLK_ENA=0
0x6C	0x0100	WSEQ_ENA=1, WSEQ_WRITE_INDEX=0_0000
0x6F	0x0100	WSEQ_ABORT=0, WSEQ_START=1, WSEQ_START_INDEX=00_0000
0x14	0x845E	TOCLK_RATE_DIV16=0, TOCLK_RATE_X4=0, SR_MODE=0, MCLK_DIV=0
0x3B	0x0039	LINEOUTL_MUTE=0, LINEOUT_VU=0, LINEOUTLZC=0, LINEOUTL_VOL=11_1001
0x3C	0x00B9	LINEOUTR_MUTE=0, LINEOUT_VU=1, LINEOUTRZC=0, LINEOUTR_VOL=11_1001
0x21	0x0000	DAC_MONO=0, DAC_SB_FILT=0, DAC_MUTERATE=0, DAC_UNMUTE_RAMP=0, DAC_OSR128=0, DAC_MUTE=0, DEEMPH=00
0x68	0x0005	CP_DYN_PWR=1

Table 3 Register Settings for DAC to Lineout Playback

PERFORMANCE PLOT



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Anlr.THD+N Ampl	Left	22Hz-22kHz, A-Weighted, Left
1	2	Blue	Solid	1	Anlr.THD+N Ampl	Left	22Hz-22kHz, A-Weighted, Right
2	1	Green	Solid	1	Anlr.THD+N Ampl	Left	22Hz-20kHz, AES17, Left
2	2	Red	Solid	1	Anlr.THD+N Ampl	Left	22Hz-20kHz, AES17, Right

System: AP2
Board: 6201-EV1-REV3 + WM8918-6201-FL32-M-REV1
Manufacturer Mark Code: DWS
Input Path: Electrical S/PDIF In
Input Signal: 997Hz, 24-bit, 256fs
Output Path: LINEOUT 100K
Supplies: AVDD=CPVDD=DBVDD=DCVDD=1V8
BW Filter: As stated in comments
Additional Filter: As stated in comments

Figure 7 Performance Plot for DAC to Lineout with 100K Load

LINE-IN TO HEADPHONE OUTPUT

The following section details board configuration for line input to headphone output.

BLOCK DIAGRAM

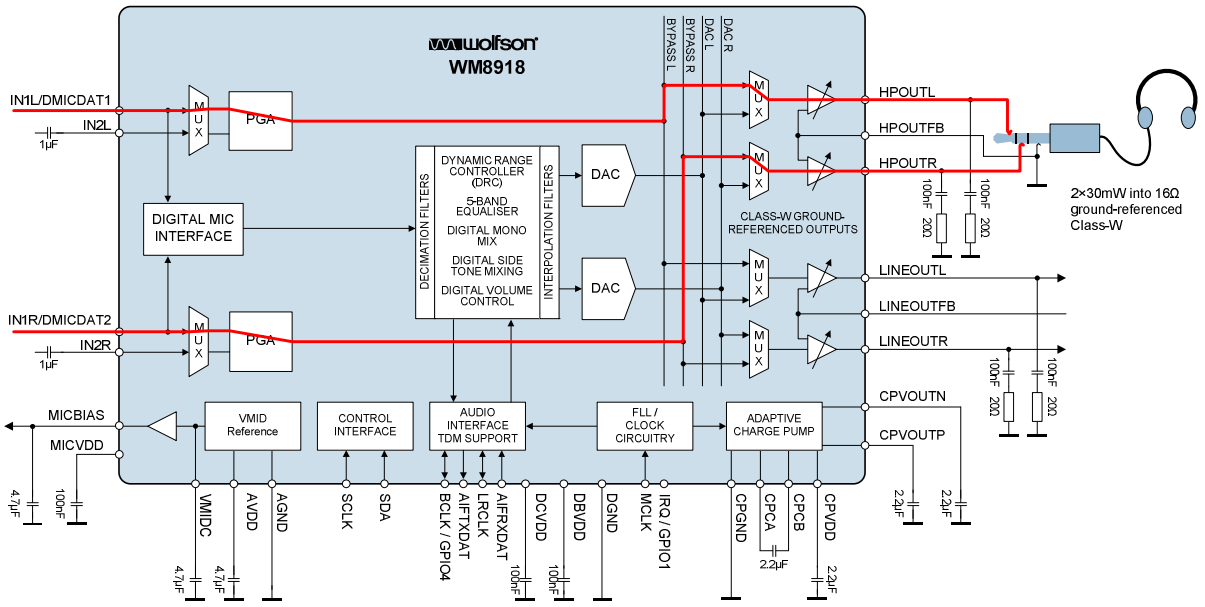


Figure 8 Path Diagram for Line Input to Headphone Playback

BOARD CONFIGURATION

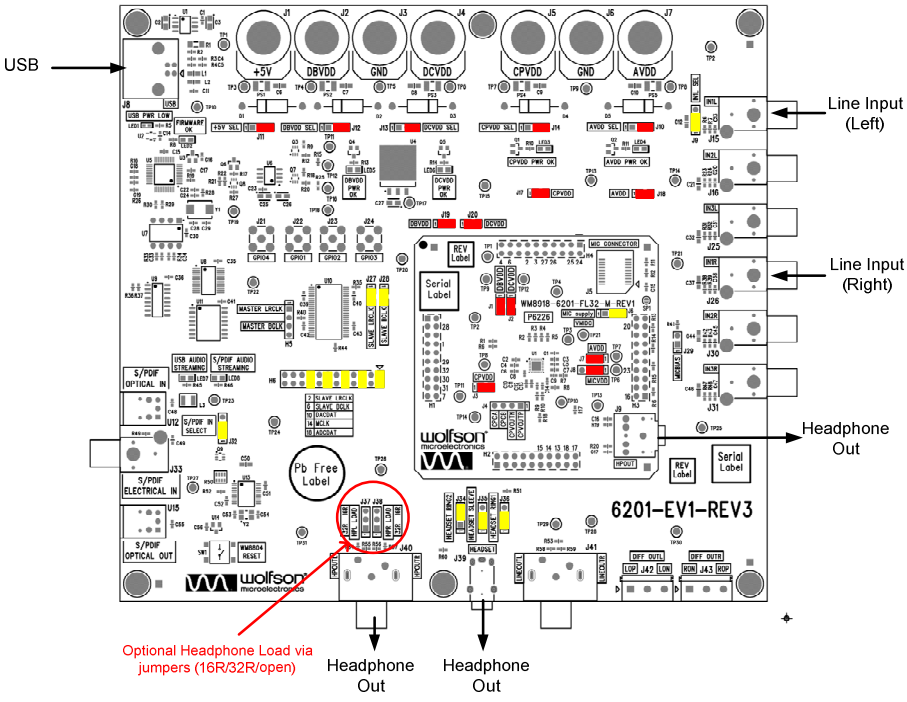


Figure 9 Board Configuration for Line In to Headphone Playback

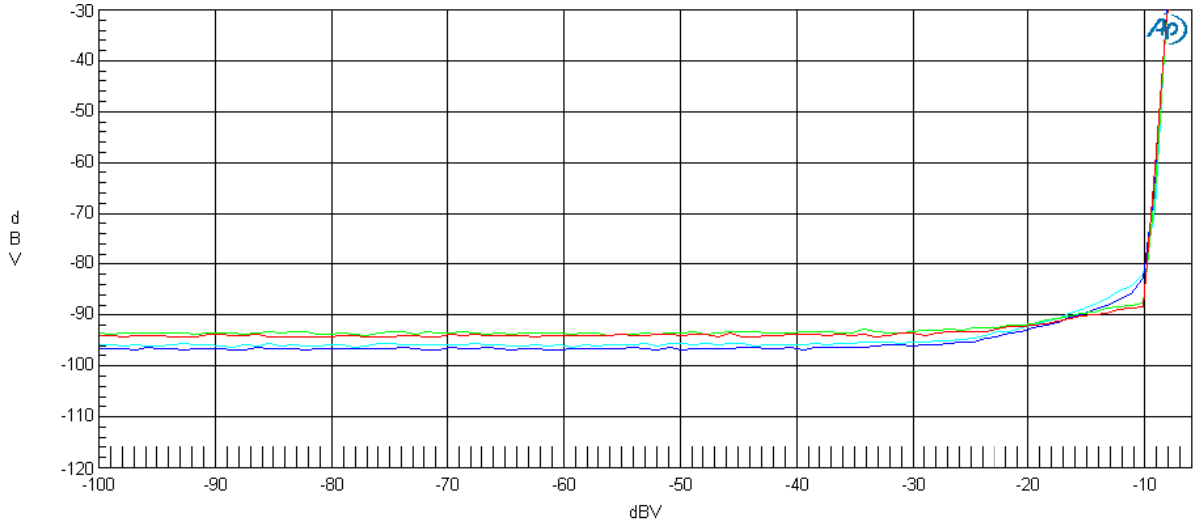
REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	Software Reset
0x04	0x0019	BIAS_ENA=1
0x05	0x0043	VMID_ENA=1; VMID_RES=01; VMID_BUF_ENA=1
0x16	0x0004	CLK_SYS_ENA=1
0x0C	0x0003	IN1L_ENA=1; IN1R_ENA=1
0x0E	0x0003	HPL_PGA_ENA=1; HPR_PGA_ENA=1
0x3D	0x000C	HPL_BYP_ENA=1; HPR_BYP_ENA=1
0x5A	0x00FF	HPL_RMV_SHORT=1; HPL_ENA_OUTP=1; HPL_ENA_DLY=1; HPL_ENA=1; HPR_RMV_SHORT=1; HPR_ENA_OUTP=1; HPR_ENA_DLY=1; HPR_ENA=1
0x62	0x0001	CP_ENA=1
0x2C	0x0005	LINMUTE=0
0x2D	0x0005	RINMUTE=0

Table 4 Register Settings for Line Input to Headphone Path

PERFORMANCE PLOT



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Anlr.THD+N Ampl	Left	22Hz-22kHz, A-weighted, Left
1	2	Blue	Solid	1	Anlr.THD+N Ampl	Left	22Hz-22kHz, A-weighted, Right
2	1	Green	Solid	1	Anlr.THD+N Ampl	Left	22Hz-20kHz, AES17, Left
2	2	Red	Solid	1	Anlr.THD+N Ampl	Left	22Hz-20kHz, AES17, Right

System: AP2
Board: 6201-EV1-REV3 + WM8918-6201-FL32-M-REV1
Manufacturer Mark Code: UZP
Input Path: IN1L/IN1R
Output Path: HPOUTL/HPOUTR (Load=32R)
Supplies: AVDD=CPVDD=DCVDD=DBVDD=1V8
BW Filter: As stated in comments
Additional Filter: As stated in comments

Figure 10 Performance Plot of Line-In to Headphone Playback with 32R Load

USB AUDIO STREAMING TO HEADPHONE PLAYBACK

The following section details board configuration for USB audio streaming to headphone output.

BLOCK DIAGRAM

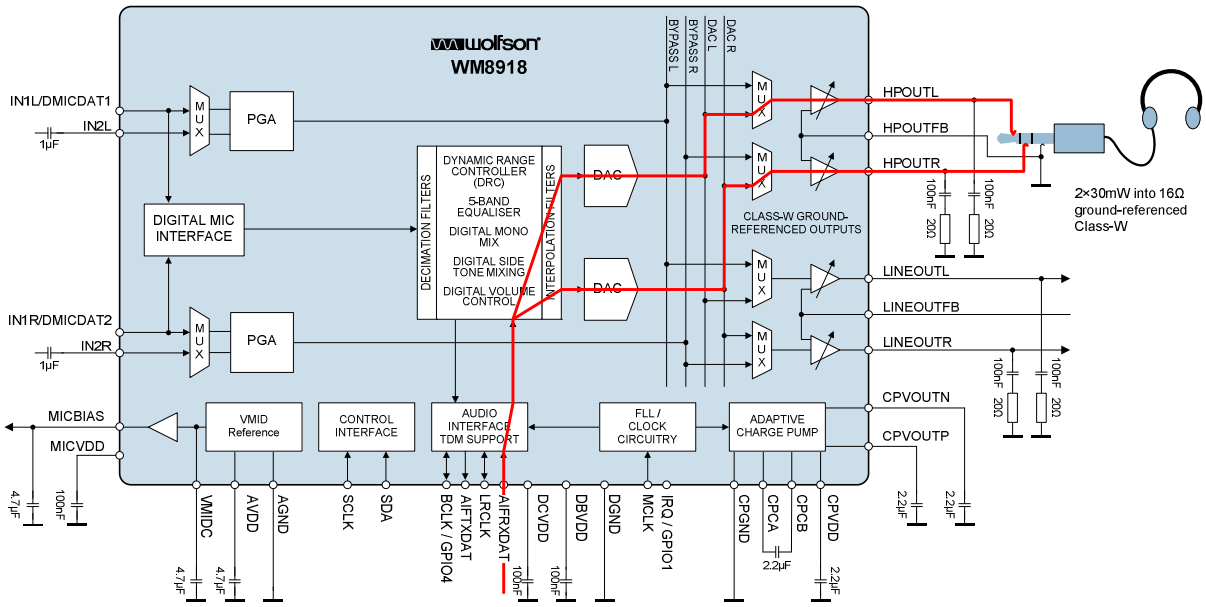


Figure 11 Path Diagram for DAC to Headphone Playback

CONFIGURATION IN MICROSOFT WINDOWS

For software configuration of USB audio streaming, please see Wolfson Application Note WAN_0240.

BOARD CONFIGURATION

The 6201-EV1-REV3 main board will automatically select audio streaming from the USB interface unless an S/PDIF input is detected. To ensure USB streaming is used, there must not be any input to either optical or electrical S/PDIF.

In the correct mode the USB Audio Streaming LED should be lit.

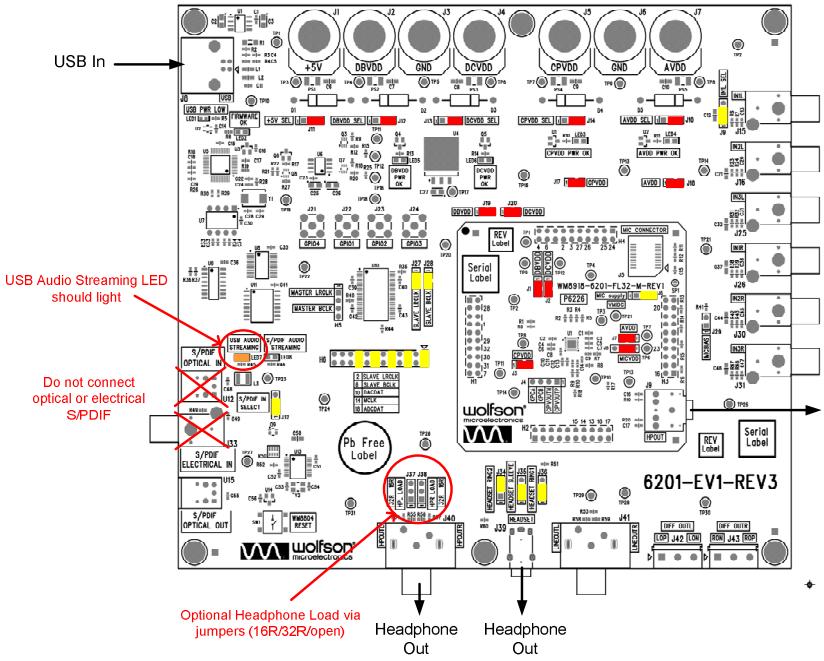


Figure 12 Board Configuration for USB Audio to Headphone

REGISTER SETTINGS

Register settings for this path are provided in Table 2.

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