

Example Configurations

DOC TYPE:	Example Configurations
BOARD REFERENCE:	WM8940-6162-FL24-M-REV3
BOARD TYPE:	Customer Mini Board
WOLFSON DEVICE(S):	WM8940
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DOC REVISION:	1.1

INTRODUCTION

The WM8940-6162-FL24-M mini-board is compatible with the 6162-EV1 customer evaluation board and together provide a complete hardware platform for evaluation of the WM8940. The WM8940 mini board can also be used independently and connected directly to a processor board using flying wires or appropriate headers. This document will cover both setups, but performance data will be based on the Wolfson system with 6162-EV1 motherboard. Configurations covered are listed below:

- DAC playback to MONOOUT
- DAC playback to 8Ω BTL speaker
- ADC record from differential microphone
- ADC record from AUX input

This document should be used as a starting point for evaluation of WM8940. It will not cover every possible usage mode.

Assumptions:

1. The user is familiar with the 6162-EV1 motherboard and that the board is configured correctly for the path of interest (see related documents below)
2. The user has setup RegWrite or WISCE as per instruction and has control of the DUT (register settings provided in this document)

Related documents:

1. WM8940-6162-FL24-M-REV3 Schematic and Layout.pdf
2. 6162-EV1 Schematic and Layout.pdf
3. WISCE Quick Start Guide.pdf

The audio interface is connected to the main board through the S/PDIF ELECTRICAL IN and S/PDIF OPTICAL OUT connectors. All control signals for the 3-wire interface to the device are through the USB interface.

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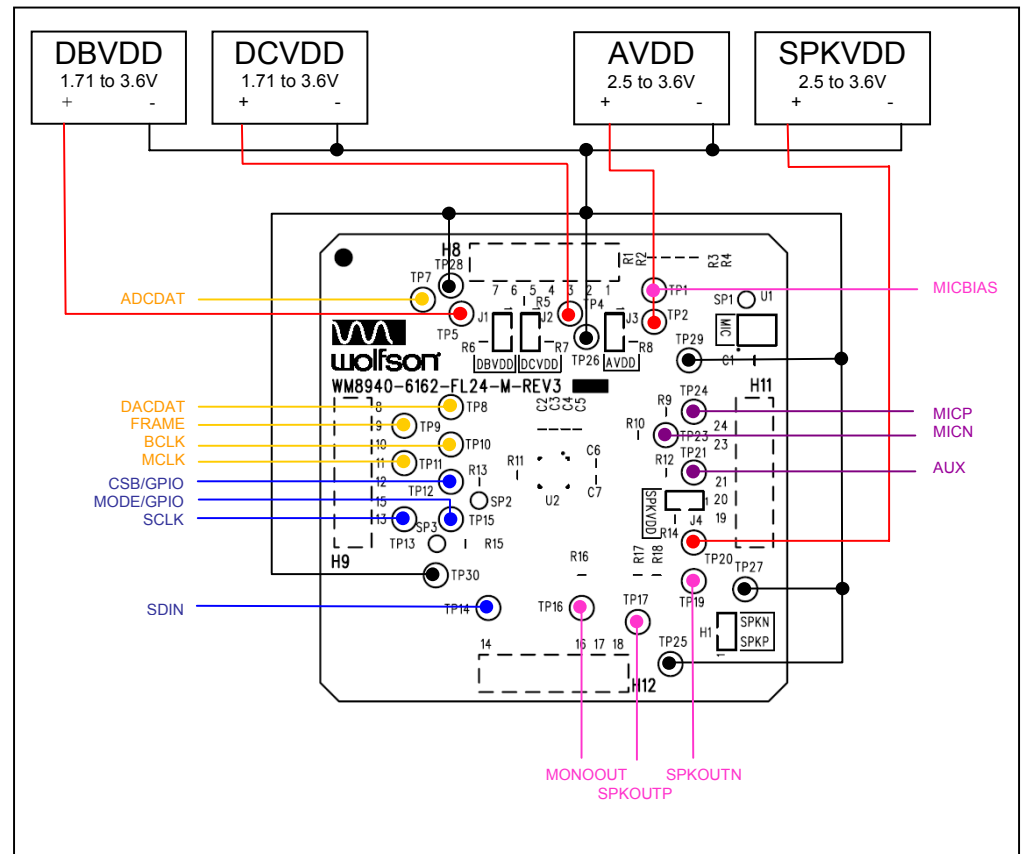
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BOARD CONFIGURATION WM8940 STAND-ALONE

The WM8940 mini board can be used as a stand-alone module for direct connection to a processor board using flying leads or dedicated headers. This section will detail important considerations and provide all information required to do this without risking damage to the device.

CONNECTION DIAGRAM

The diagram below shows the connections required to power up and control the WM8940 mini board.



I/O TABLE

SIGNAL	BOARD REFERENCE	HEADER	IMPORTANT NOTES
Voltage Supplies			
AVDD	TP2	H8 pin 4	AVDD = 2.5V to 3.6V
SPKVDD	TP20	H11 pin 6	SPKVDD = 2.5V to 3.6V
DCVDD	TP4	H8 pin 8	DCVDD = 1.71V to 3.6V but must be less than or equal to AVDD, SPKVDD and DBVDD
DBVDD	TP5	H8 pin 10	DBVDD = 1.71V to 3.6V
Ground			
AGND	Common GND on any of TP25, TP26, TP27, TP28, TP29 and TP30	H9, H11, H12 odd numbered pins	Analogue and digital grounds must be within 0.3V of each other
SPKGND			
DGND			
Control Interface			
MODE/GPIO	TP15 (Controlled using SP3 on board)	H9 pin 12	2-wire (default): MODE to GND via R15 3-wire: MODE to DBVDD via SP3
CSB/GPIO	TP12 (Controlled using SP2 on board)	H9 pin 10	2-wire address 0x34 (default): CSB to GND via R13 2-wire address 0x36: CSB to DBVDD via SP2
SDIN	TP14	H12 pin 2	All control interface signals should swing between DGND and DBVDD
SCLK	TP13	H9 pin 14	
Master Clock			
MCLK	TP11	H9 pin 8	Signal should swing between DGND and DBVDD
Audio Interface			
BCLK	TP10	H9 pin 6	All audio interface signals should swing between DGND and DBVDD
FRAME	TP9	H9 pin 4	
DACDAT	TP8	H9 pin 2	
ADCDAT	TP7	H8 pin 14	
Analogue Inputs			
MICN	TP23	H11 pin 12	Full scale swing should not exceed AVDD/3.3 Vrms single-ended (L/RIN). Pseudo-differential full scale swing should not exceed AVDD*0.7/3.3 Vrms
MICP	TP24	H11 pin 14	
AUX	TP21	H11 pin 8	Full scale swing should not exceed AVDD/3.3 Vrms
Analogue Outputs			
MICBIAS	TP1	H8 pin 2	MBVSEL=0 sets bias voltage to 0.9*AVDD, MBVSEL=1 sets bias voltage to 0.65*AVDD. Max current 3mA.
MONOOUT	TP16	H12 pin 12	Line output or mono headphone
SPKOUTP	TP17	H12 pin 14	+ve terminal of BTL speaker output
SPKOUTN	TP19	H11 pin 4	-ve terminal of BTL speaker output

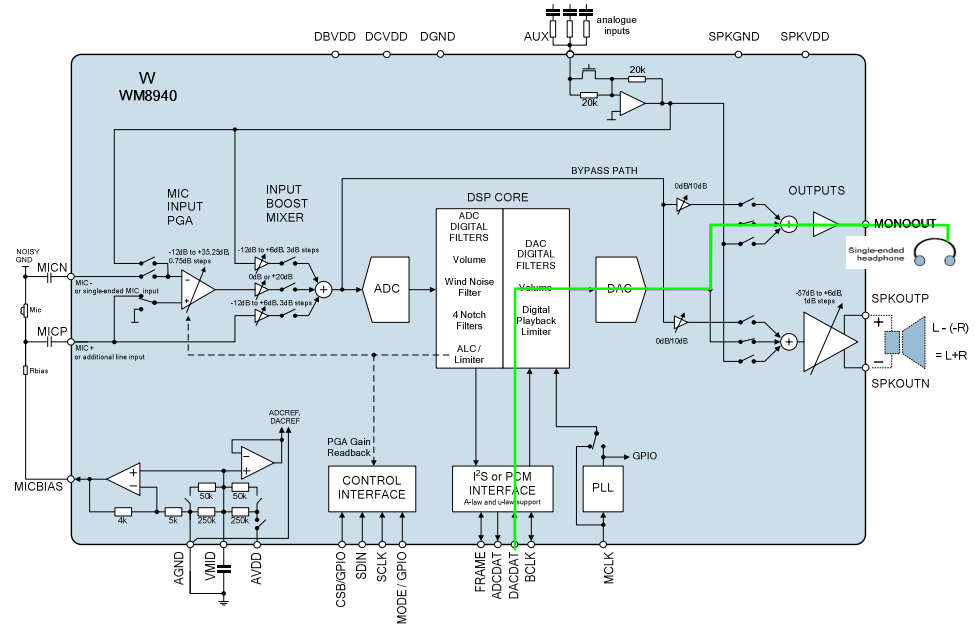
BOARD CONFIGURATION USING 6162-EV1 MAIN BOARD

This section focuses on evaluation of the WM8940 mini board in combination with the 6162-EV1 main board. This “system” is the reference platform for measurement data contained in this document. Please note that only a limited number of usage modes will be covered.

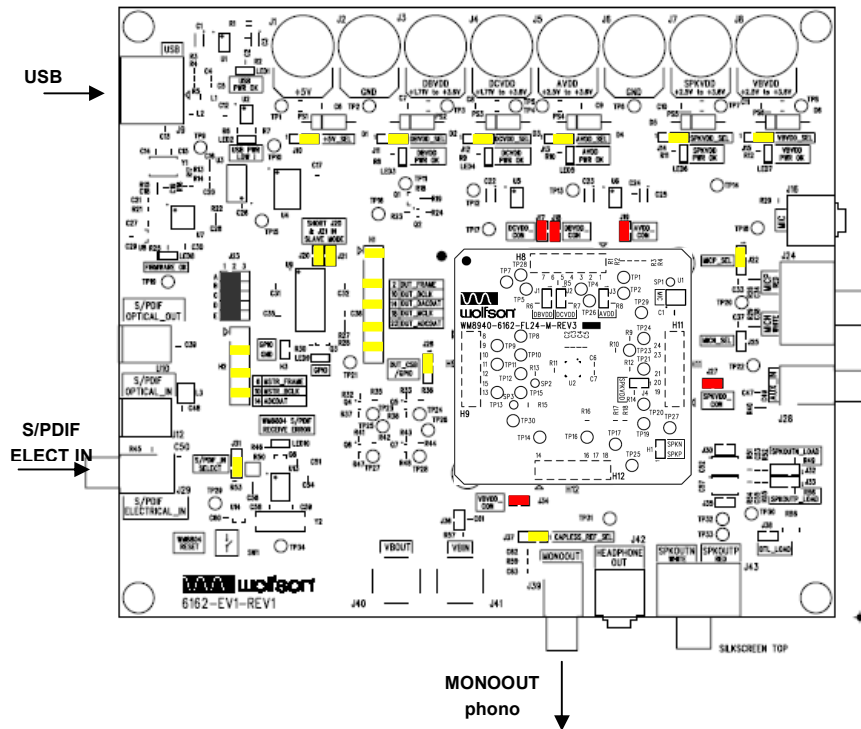
DAC PLAYBACK TO MONOOUT

The following section details board configuration for mono DAC playback to MONOOUT.

EVALUATION BOARD SETUP



BOARD CONFIGURATION



REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised for pops and clicks.

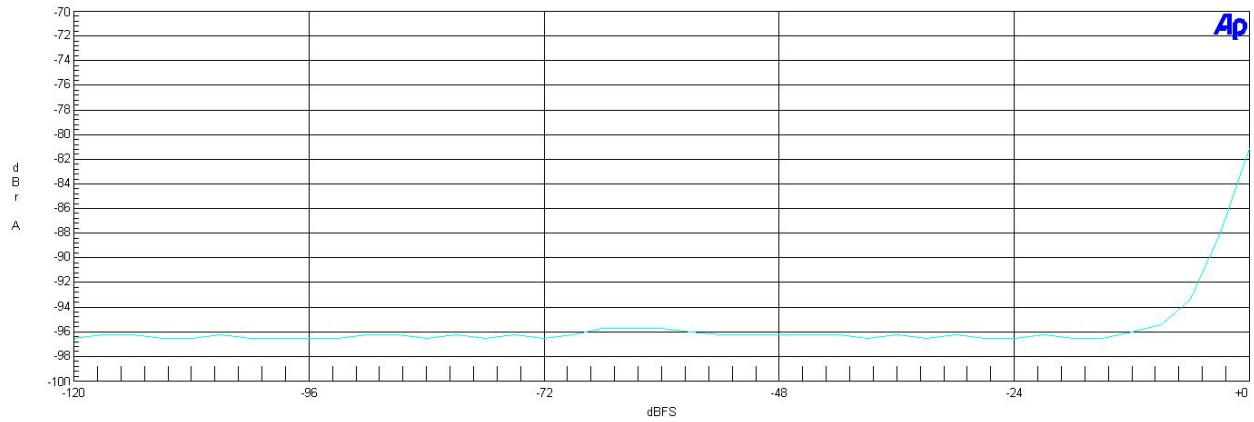
REG INDEX	DATA VALUE	COMMENT
R0	0x000	Reset (all registers to default setting)
R1	0x08D	LVLSHIFT_EN On, BIASEN On, BUFI0EN On, VMIDSEL = 50k
R3	0x0ED	MONOEN On, SPKNEN On, SPKPEN On, VBUFEN Off, MONOMIX On, SPKMIXEN On, DACEN On
R6	0x000	CLKSEL=MCLK, BCLK=MCLK, MCLKDIV=1, MS=Slave
R49	0x002	TSDEN On, VROI=1k
R56	0x001	MONOATTN=0dB, DAC2MONO selected

THD+N V AMPLITUDE PERFORMANCE CURVE

Wolfson Microelectronics plc

WM8941-EV1 -- DAC THD+N v Amplitude -- DAC Default Settings

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Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Anlr.THd+N Ampl	Left	

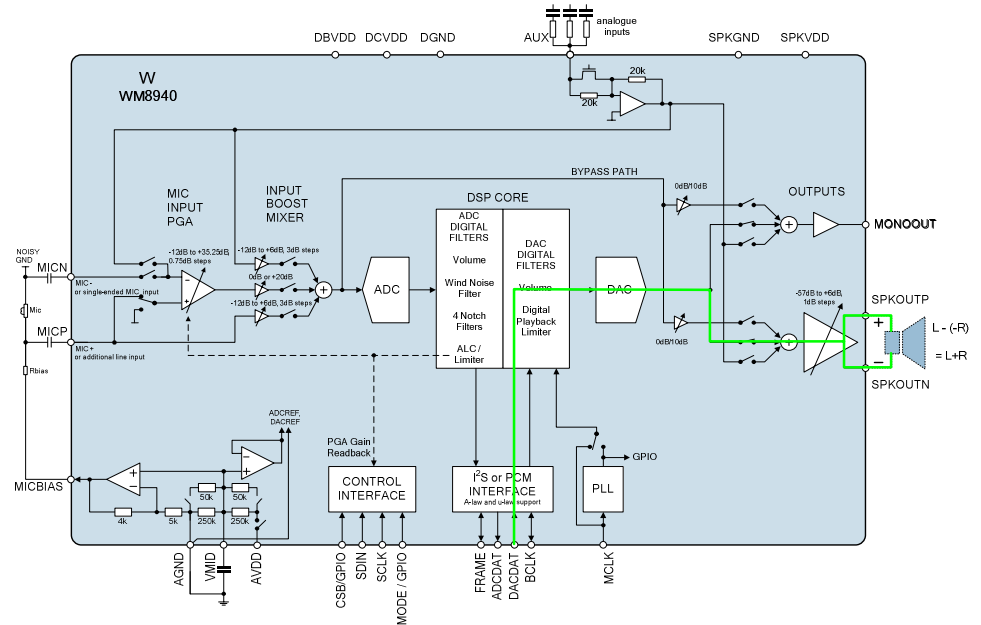
System AP2
 Template Revision: 1.0
 Board Revision: 1.0
 Device Date Code: 63AASJ4
 Input Path: SPDIF_IN
 Input Signal: 997Hz, 0dBFS, 24-bit, 256fs (fs=48kHz)
 Output Path: Headphone Out
 Output Reference: +0.619dBuA
 Supplies: AVDD=DEVDD=HPVDD=+3.3V, DCVDD=+1.5V
 BW filter: 22Hz - 22kHz
 Additional Filtering: A-weighting
 Dither: None
 RMS or Averaging: Averaging

DAC_THD+N_vs_Amplitude_SPDIF_In_to_MONOOUT_48kHz.at27

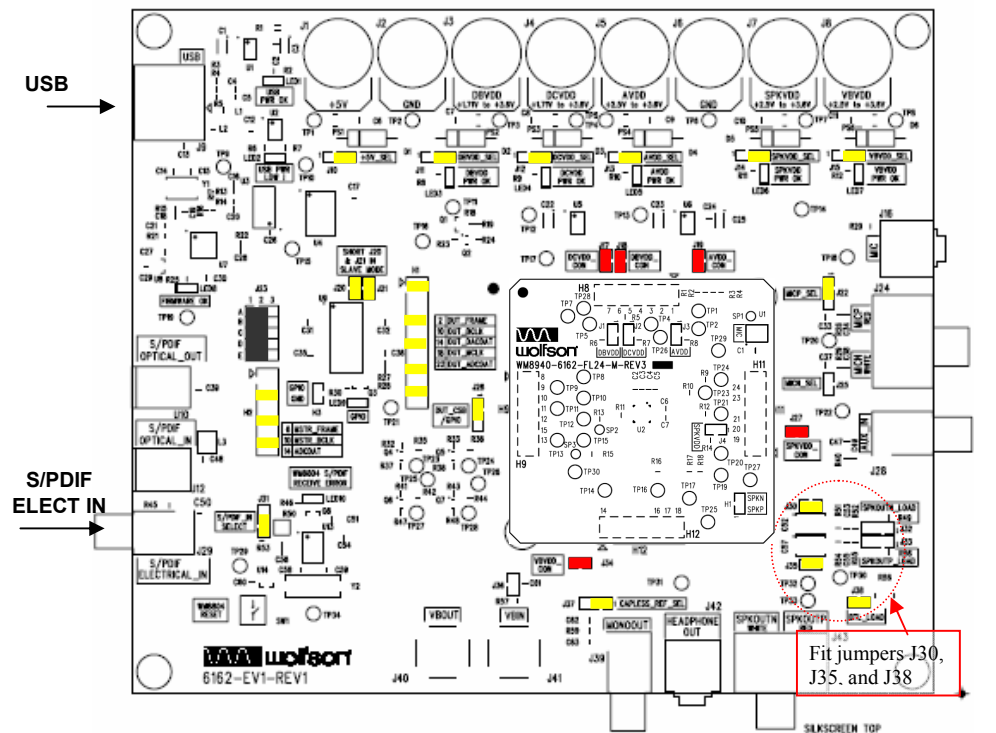
DAC PLAYBACK TO 8Ω BTL SPEAKER

The following section details board configuration for mono DAC playback to 8Ω BTL speaker on SPKOUTP and SPKOUTN.

EVALUATION BOARD SETUP



BOARD CONFIGURATION



SPKOUTN/P
Phono
AP2 CHA+ to White
AP2 CHA- to Red

REGISTER SETTINGS

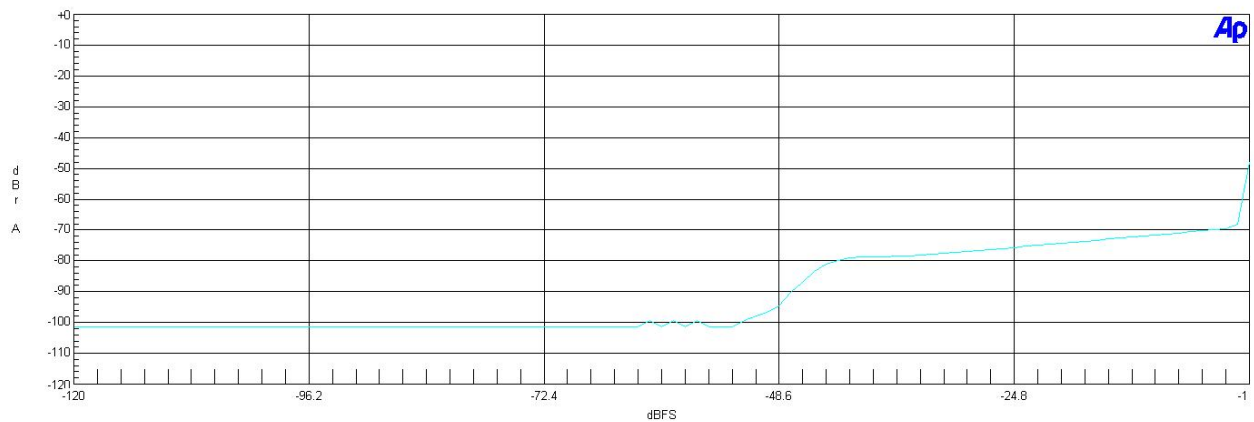
REG INDEX	DATA VALUE	COMMENT
R0	0x000	Reset (all registers to default setting)
R1	0x08D	LVLSHIFT_EN On, BIASEN On, BUFIOEN On, VMIDSEL = 50k
R3	0x0ED	MONOEN On, SPKNEN On, SPKPEN On, VBUFEN Off, MONOMIX On, SPKMIXEN On, DACEN On
R6	0x000	CLKSEL=MCLK, BCLK=MCLK, MCLKDIV=1, MS=Slave
R49	0x002	TSDEN On, VROI=1k
R50	0x001	DAC2SPK selected
R54	0x039	SPKATTN=0dB, Speaker output enabled, SPKVOL=0dB

THD+N V AMPLITUDE PERFORMANCE CURVE

Wolfson Microelectronics plc

WM8941-EV1 -- DAC THD+N v Amplitude -- DAC Default Settings

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Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Anlr.THd+N Ampl	Left	

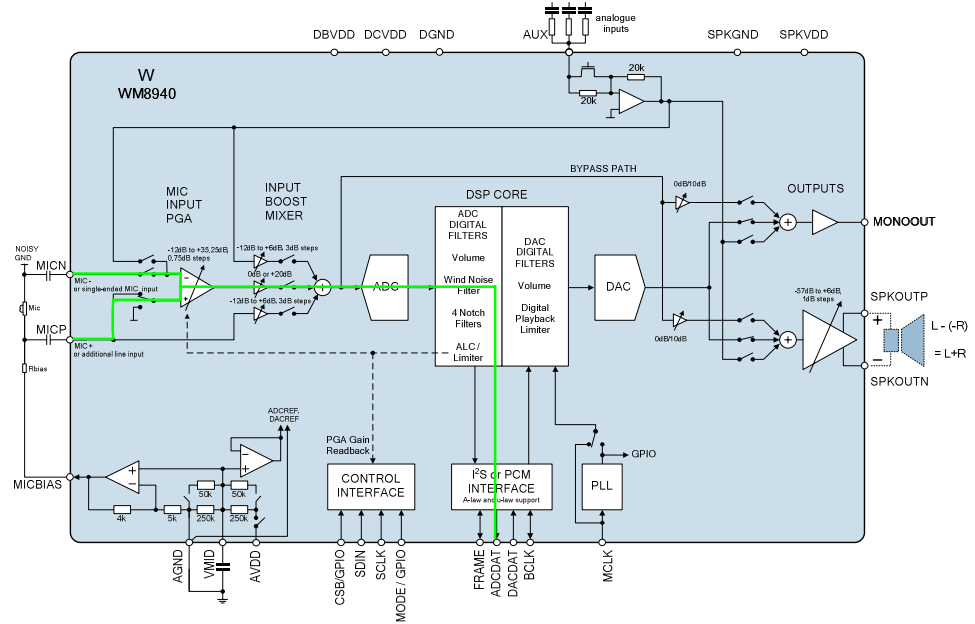
System: AP2
 Template Revision: 1.0
 Board Revision: 1.0
 Device Date Code: 63AASJ4
 Input Path: SPDIF_IN
 Input Signal: 997Hz, 0dBFS; 24-bit; 256fs (fs=48kHz)
 Output Path: LROUT1
 Output Reference: +0.6694BrA
 Supplies: AVDD=DBVDD=HPVDD=+3.3V, DCVDD=+1.5V
 BW filter: 22kHz - 22kHz
 Additional Filtering: A-weighting
 Dither: None
 RMS or Averaging: Averaging

DAC_THD+N_vs_Amplitude_SPDIF_In_to_SPKOUT_8ohmBTL_48kHz.at27

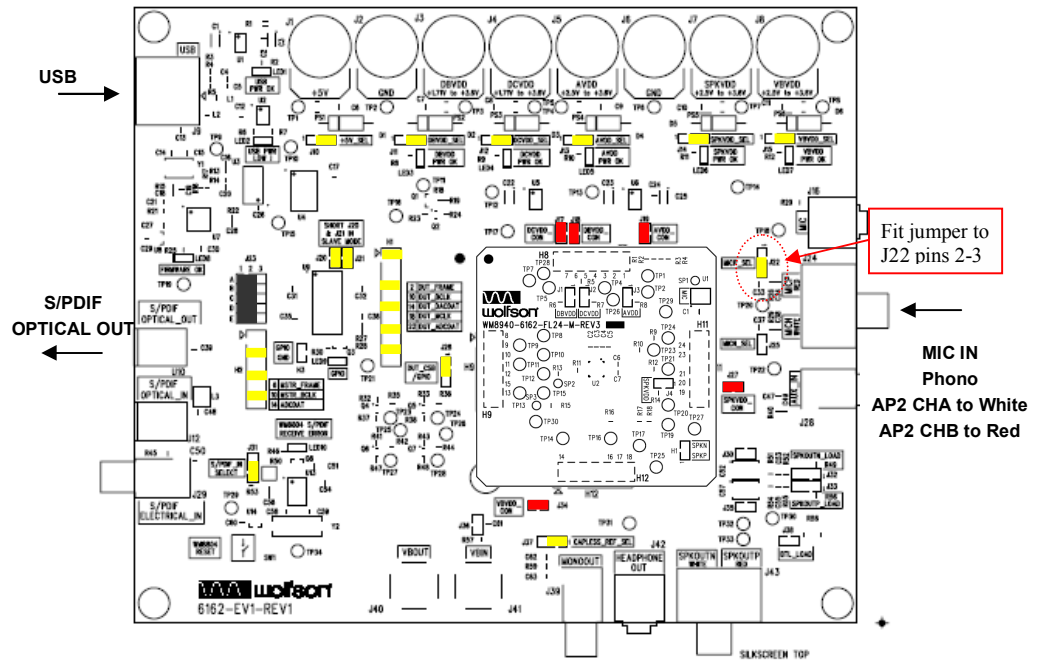
MICN-MICP TO ADC

The following section details board configuration for connecting a differential Microphone to MICN and MICP and to the mono ADC.

EVALUATION BOARD SETUP



BOARD CONFIGURATION



REGISTER SETTINGS

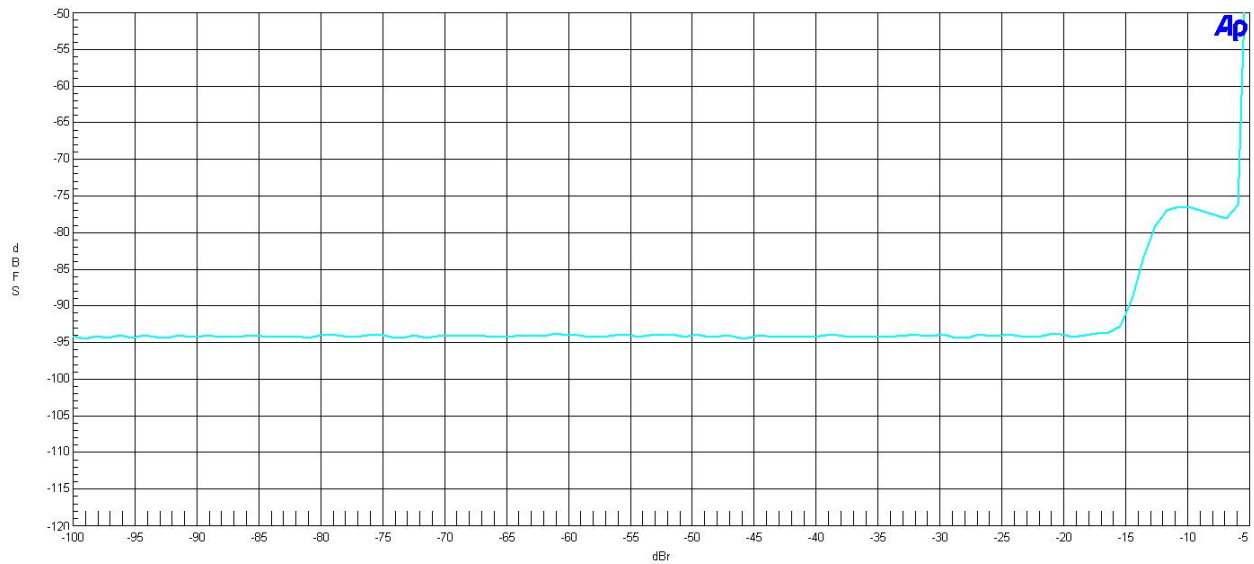
REG INDEX	DATA VALUE	COMMENT
R0	0x000	Reset (all registers to default setting)
R1	0x08D	LVLSHIFT_EN On, BIASEN On, BUFOEN On, VMIDSEL = 50k
R2	0x015	BOOSTEN On, INPPGAEN On, ADCEN On
R6	0x000	CLKSEL=MCLK, BCLK=MCLK, MCLKDIV=1, MS=Slave
R44	0x003	MBVSEL=0.9*AVDD, MICN2INPPGA to PGA -ve terminal, MIC2INPPGA to PGA +ve terminal
R45	0x010	INPPGA enabled, INPPGAVOL=0dB
R47	0x000	PGABOOST=0dB
R49	0x002	TSDEN On, VROI=1k

THD+N v AMPLITUDE PERFORMANCE CURVE

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WM8941-EV1 -- ADC THD+N v Amplitude -- ADC Default Settings

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Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	2	DSP Anlr:THD+N Ampl A	Left	

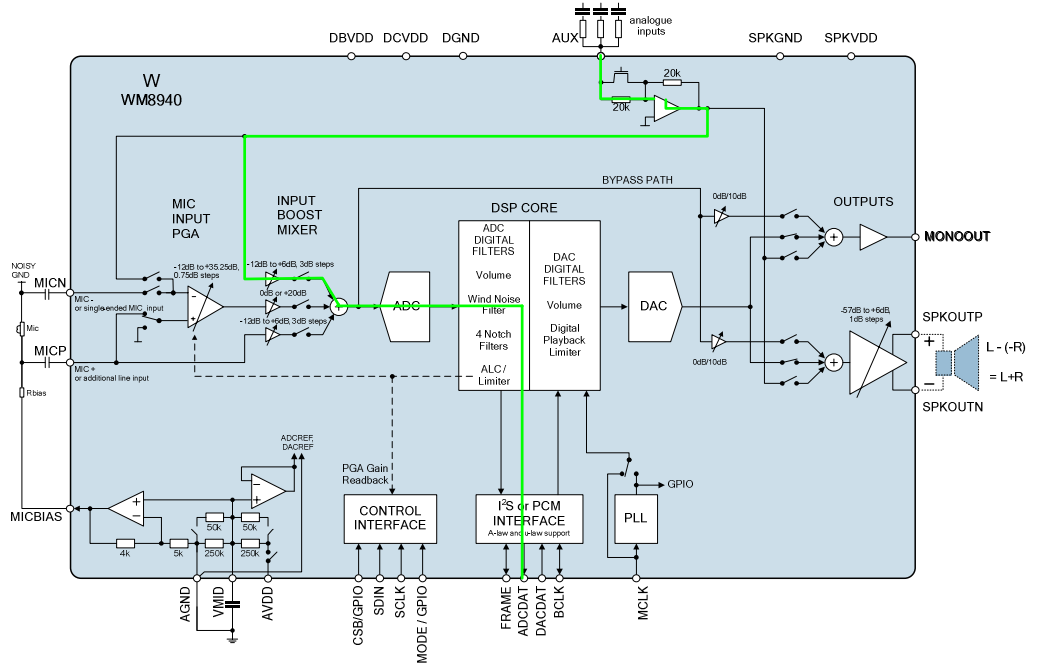
Test System: AP2
 Template Revision: 1.0
 Board Revision: 1.0
 Device Date Code: 63AASJ4
 Input Path: LINE_IN
 Input Signal: 0.997kHz, 0dB
 Input Reference: 0dBV
 Output Path: SPIDIF_OUT
 Output Signal: 24 bit, 48kHz (256fs)
 Supplies: AVDD=DBVDD=HPVDD=+3.3V, DCVDD=+1.5V
 BW Filtering: 22Hz - 20kHz
 Additional Filtering Type: A-weighting
 RMS or Averaging: RMS

ADC_THD+N_vs_Amplitude_Diff_MICIN_to_SPDIF_48kHz.at27

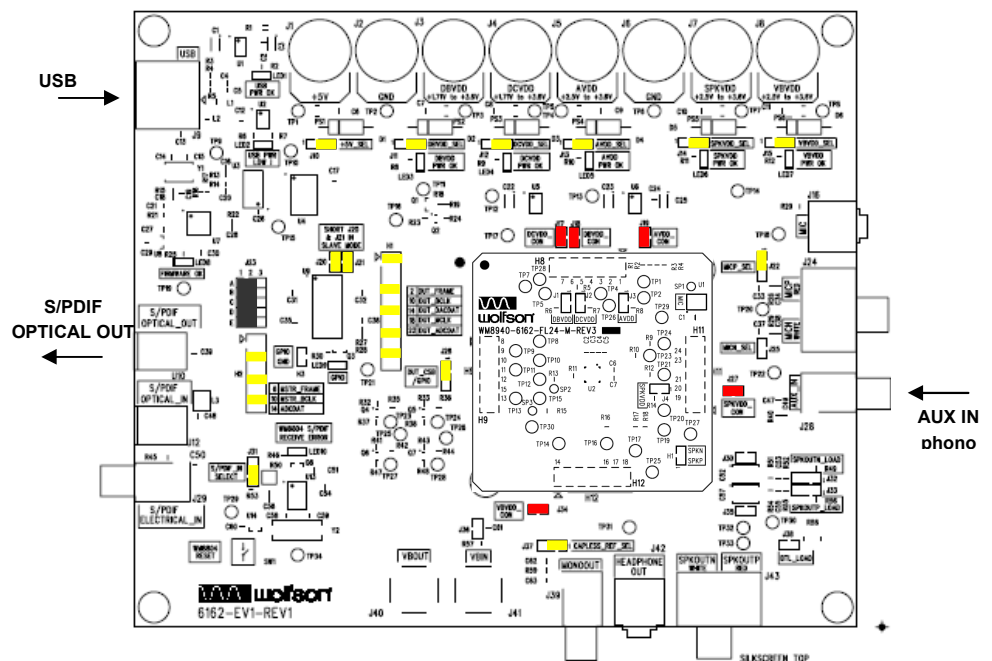
AUX TO ADC

The following section details board configuration for connecting AUX input to the mono ADC bypassing the PGA.

EVALUATION BOARD SETUP



BOARD CONFIGURATION



REGISTER SETTINGS

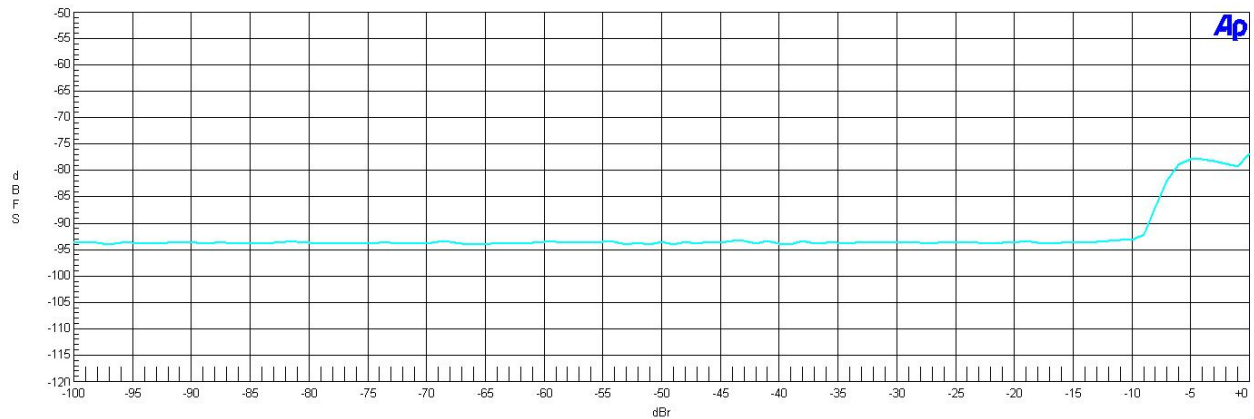
REG INDEX	DATA VALUE	COMMENT
R0	0x000	Reset (all registers to default setting)
R1	0x08D	LVLSHIFT_EN On, BIASEN On, BUFIOEN On, VMIDSEL = 50k
R2	0x015	BOOSTEN On, INPPGAEN On, ADCEN On
R6	0x000	CLKSEL=MCLK, BCLK=MCLK, MCLKDIV=1, MS=Slave
R44	0x000	Bypass PGA
R45	0x010	INPPGA enabled, INPPGAVOL=0dB
R47	0x007	AUXBOOSTVOL=0dB
R49	0x002	TSDEN On, VROI=1k

THD+N V AMPLITUDE PERFORMANCE CURVE

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WM8941-EV1 -- ADC THD+N v Amplitude -- ADC Default Settings

09/20/07 11:28:50



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	2	DSP Anlr THD+N Ampl A	Left	

Test System: AP2
 Template Revision: 1.0
 Board Revision: 1.0
 Device Date Code: 63AASJ4
 Input Path: LINE_IN
 Input Signal: 0.997kHz, 0dB
 Input Reference: 0dBV
 Output Path: S/PDIF_OUT
 Output Signal: 24 bit, 48kHz (256fs)
 Supplies: AVDD=BBVDD=HPVDD=+3.3V, DCVDD=+1.5V
 BW Filtering: 22Hz - 20kHz
 Additional Filtering Type: A-weighting
 RMS or Averaging: RMS

ADC_THD+N_vs_Amplitude_AUX_to_SPDIF_48kHz.at27

APPLICATIONS SUPPORT

If you require more information or require technical support, please contact the Wolfson Microelectronics Applications group through the following channels:

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