WM8956-6158-FL32-M-REV1
Example Configurations

DOC TYPE:	EXAMPLE CONFIGURATIONS
BOARD REFERENCE:	WM8956-6158-FL32-M-REV1
BOARD TYPE:	Customer Mini Board
WOLFSON DEVICE(S):	WM8956
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INTRODUCTION

The WM8956-6158-FL32-M-REV1 Customer Mini Board is compatible with the 6158-EV1 customer evaluation board and together provide a complete hardware platform for evaluation of the WM8956. The WM8956 Customer Mini Board can also be used independently and connected directly to a processor board using flying wires or appropriate headers. This document will cover both, but performance data will be based on the Wolfson system with 6158-EV1 main board. Configurations covered are listed below:

- DAC Playback to headphone on HP_L/R
- Analogue bypass from L/RINPUT3 to 16Ω headphone on HPL/HPR
- DAC playback to 8Ω speaker (Mini board)

This document should be used as a starting point for evaluation of WM8956 but it will not cover every possible configuration.

Assumptions:

1. The user is familiar with the 6158-EV1 main board and the board is configured correctly for the path of interest (see related documents below)
2. The user has set up WISCE as per instruction and has control of the DUT (register settings provided in this document)

Related documents:

1. WM8956-6158-FL32-M_Schematic_Layout_rev_1.0.pdf
2. 6158-EV1-REV1_Schematic_Layout.pdf
3. WISCE Quick Start Guide.pdf

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BOARD CONFIGURATION STAND-ALONE

The WM8956 Customer Mini Board can be used a stand-alone module for direct connection to a processor board via flying leads or dedicated headers. This section will detail important considerations and provide all information required to do this without risking damage to the device.

CONNECTION DIAGRAM

Figure 1 below shows the connections required to power-up and control the WM8956 Customer Mini Board.

Please refer to Table 1 for further details on external I/O connections. Table 2 contains a list of all shorting points.
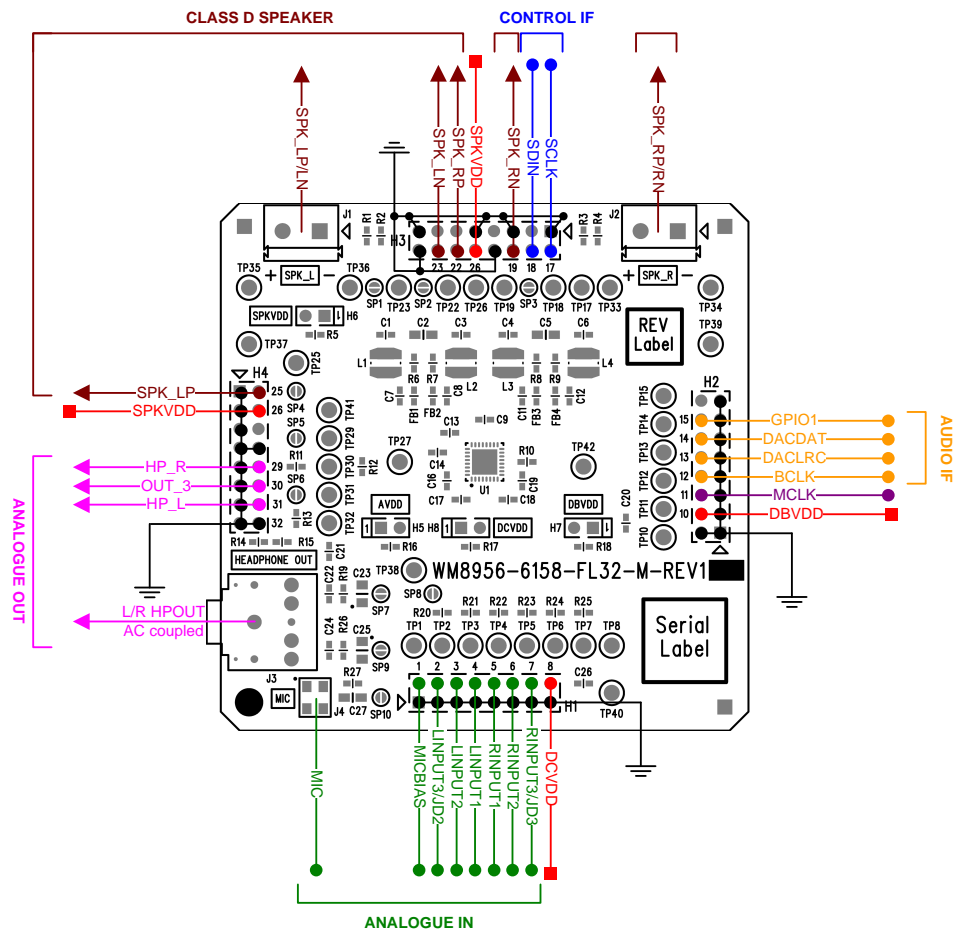

Figure 1 Stand-Alone Board Configuration

I/O TABLE

SIGNAL	BOARD REFERENCE	IMPORTANT NOTES
Voltage Supplies		
AVDD	H4: pin 16	AVDD = 2.7V to 3.6V AVDD must be less or equal to SPKVDD1 and SPKVDD2
DBVDD	H2: pin 4	DBVDD = 1.71V to 3.6V
DCVDD	H1: pin 16	DCVDD = 1.71V to 3.6V DCVDD must be less than or equal to AVDD and DBVDD
SPKVDD1 SPKVDD2	Common supply: H3: pin 10, H4: pin 4	SPKVDD = 2.7V to 5.5V
Ground		
DGND SPKGND1 SPKGND2 AGND	Common GND: H2: pin 2, H3: pin 8, H3: pin 16, H4: pin 8	Analogue, digital and speaker grounds must always be within 0.3V of each other
Control Interface		
SCLK	H3: pin 2	All control interface signals should swing between DGND and DBVDD
SDIN	H3: pin 4	
Master Clock		
MCLK	H2: pin 6	Signal should swing between DGND and DBVDD
Audio Interface		
BCLK	H2: pin 8	All audio interface signals should swing between DGND and DBVDD
DACLRC	H2: pin 10	
DACDAT	H2: pin 12	
GPIO1	H2: pin 14	
Analogue Inputs		
LINPUT1	H1: pin 8	Full scale swing should not exceed AVDD/3.3 Vrms
LINPUT2	H1: pin 6	
LINPUT3/JD2	H1: pin 4	
RINPUT1	H1: pin 10	
RINPUT2	H1: pin 12	
RINPUT3/JD3	H1: pin 14	
Analogue Outputs		
MICBIAS	H1: pin 2	Microphone Bias
VMID	TP27	Midrail voltage decoupling capacitor
SPK_RN	H3: pin 6	Right speaker negative output (unfiltered)
	TP19	Right speaker negative output (low-pass filtered)
SPK_RP	H3: pin 12	Right speaker positive output (unfiltered)
	TP22	Right speaker positive output (low-pass filtered)
SPK_LN	H3: pin 14	Left speaker negative output (unfiltered)
	TP23	Left speaker negative output (low-pass filtered)
SPK_LP	H4: pin 2	Left speaker positive output (unfiltered)
	TP25	Left speaker positive output (low-pass filtered)
HP_L	H4: pin 14	HP output (left channel) or left channel of AC coupled HP Jack (J3)
HP_R	H4: pin 10	HP output (right channel) or right channel of AC coupled HP Jack (J3)
OUT3	H4: pin 12	Mono, left, right or buffered midrail output for capless mode

Table 1 I/O Configuration

SHORTING POINTS TABLE

REFERENCE	FUNCTION
SP1	Short SP1 to connect SPK_LN to main board via H3
SP2	Short SP2 to connect SPK_RN to main board via H3
SP3	Short SP3 to connect SPK_RP to main board via H3
SP4	Short SP4 to connect SPK_LP to main board via H4
SP5	Short SP5 to connect HPR to main board via H4
SP6	Short SP6 to connect HPL to main board via H4
SP7	Short SP7 to bypass C23 (for cap-less headphone mode)
SP8	Short SP8 for jack detect via LINPUT3/JD2
SP9	Short SP9 to bypass C25 (for cap-less headphone mode)
SP10	Short SP10 to connect the SM mic to the DUT via LINPUT1

Table 2 List of Shorting Points

BOARD CONFIGURATION WITH 6158-EV1-REV1 MAIN BOARD

This section focuses on evaluation of the WM8956-6158-FL32-M-REV1 Customer Mini Board in combination with the 6158-EV1 main board. This system is the reference platform for measurement data contained in this document. Please note that only a limited number of usage modes will be covered.
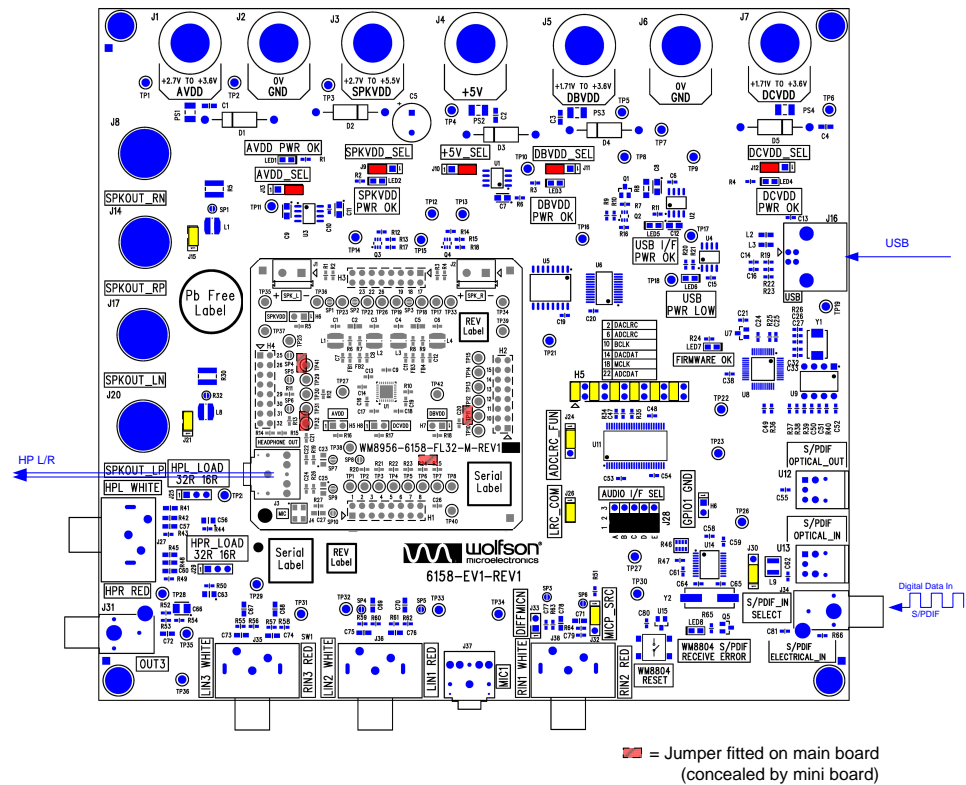
DAC PLAYBACK TO HEADPHONE ON HP_L/R

The following section details board configuration for DAC Playback to headphone on HP_L/R.

BLOCK DIAGRAM
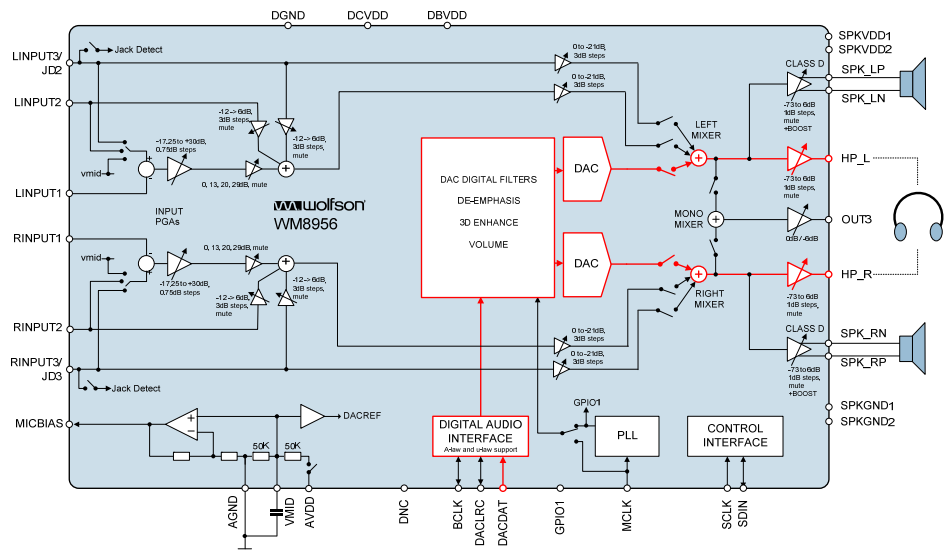
BOARD CONFIGURATION

= Jumper fitted on main board
(concealed by mini board)

REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

REG INDEX	DATA VALUE	COMMENT
R15	0x000	Reset
R25	0x0C0	VMID=50K, Enable VREF
R26	0x1E0	Enable DACL, DACR, LOUT1 and ROUT1
R47	0x00C	Enable left output mixer and right output mixer
R34	0x100	Left DAC to left output mixer enabled (LD2LO), 0dB
R37	0x100	Right DAC to right output mixer enabled (RD2RO), 0dB
R2	0x179	LOUT1 Vol = 0dB, volume update enabled
R3	0x179	ROUT1 Vol = 0dB, volume update enabled
R5	0x000	Unmute DAC digital soft mute

PERFORMANCE PLOT

WM8956-6158-FL32-M-REV1 -- DAC-HP THD+N v Amplitude
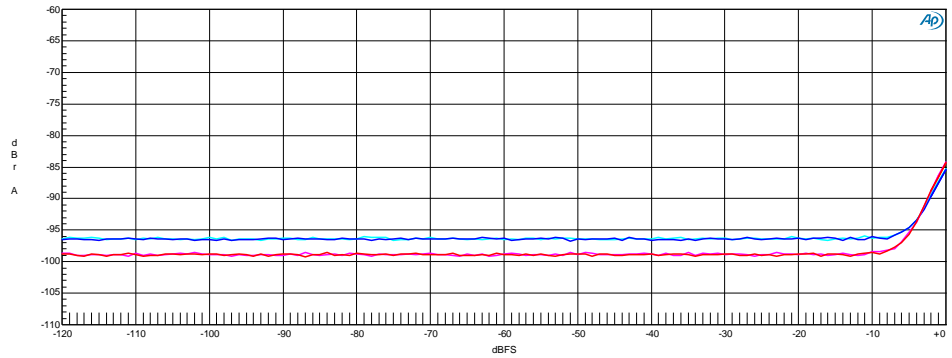
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	2	Anlr.THD+N Ampl	Left	HPL
1	2	Blue	Solid	2	Anlr.THD+N Ampl	Left	HPR
2	1	Magenta	Solid	2	Anlr.THD+N Ampl	Left	HPL A-weight
2	2	Red	Solid	2	Anlr.THD+N Ampl	Left	HPR A-weight

System AP2
Board: WM8956-6158-FL32-M-REV1-S
Device Date Code: 79AADUT
Input Path: SPDIF_IN
Input Signal: 997Hz; 0dBFS; 24-bit; 256fs (fs=48kHz)
Output Path: HP_L/R
Output Reference: -0.069 dBV
Supplies: AVDD=DBVDD=DCVDD=+3.3V
BW filter : 22Hz - 20kHz
Additional Filtering: As stated
Dither: None
RMS or Averaging: Averaging
Load = 10kOhm

DAC_THD+N_vs_Amplitude_to_HPLR_48kHz.at27

ANALOGUE BYPASS FROM L/RINPUT3 TO 16Ω HEADPHONE ON HPL/HPR

The following section details board configuration for Analogue bypass from L/RINPUT3 to 16Ω headphone on HPL/HPR.
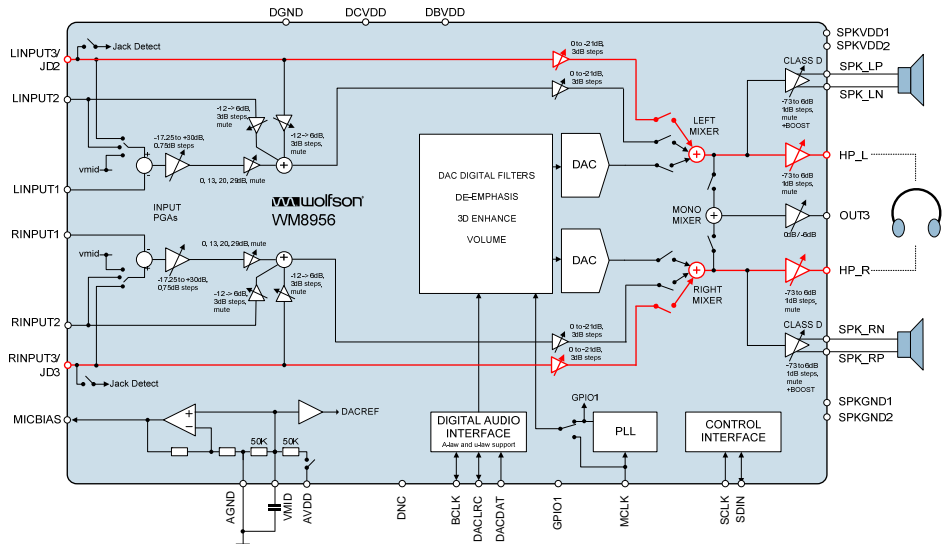
BLOCK DIAGRAM

BOARD CONFIGURATION

= Jumper fitted on main board
(concealed by mini board)
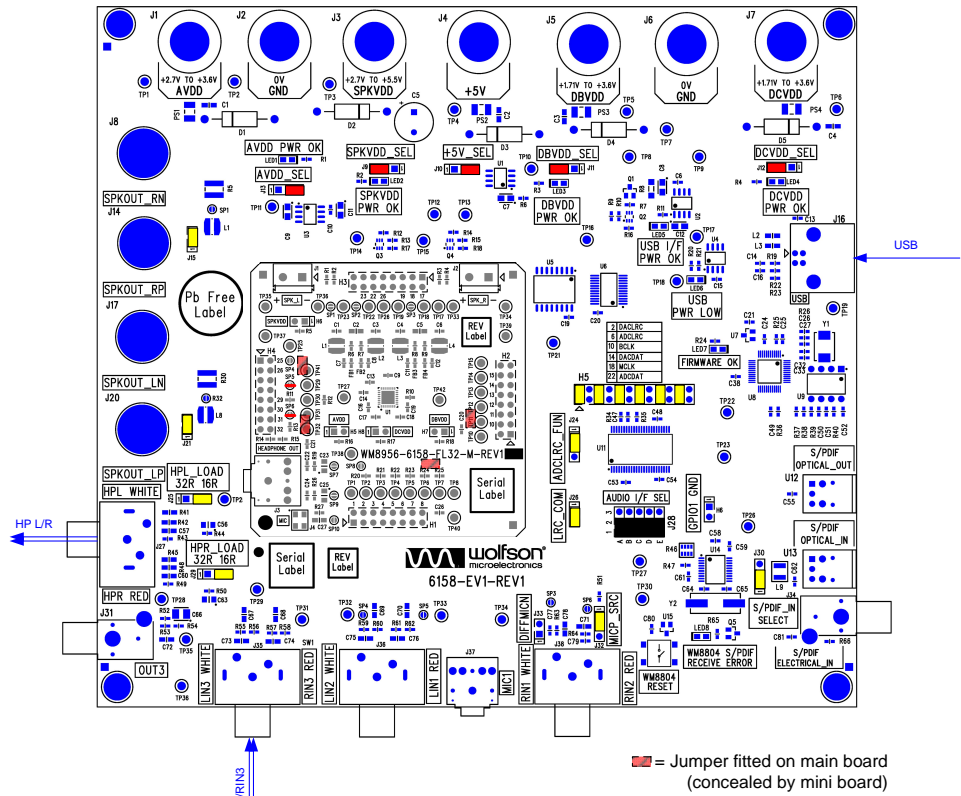
REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

REG INDEX	DATA VALUE	COMMENT
R15	0x000	Reset
R25	0x0F0	VMID=50K, Enable VREF, AINL and AINR
R26	0x060	Enable LOUT1 and ROUT1
R32	0x000	LINPUT1 not connected to PGA (LMN1)
R33	0x000	RINPUT1 not connected to PGA (RMN1)
R47	0x00C	Enable left and right channel input PGA
R34	0x080	Enable LINPUT3 to left output mixer (LI2LO), LINPUT3 to Left mixer vol = 0dB
R37	0x080	Enable RINPUT3 to right output mixer (RI2RO), RINPUT3 to Right mixer vol = 0dB
R2	0x179	LOUT1 Vol = 0dB, volume update enabled
R3	0x179	ROUT1 Vol = 0dB, volume update enabled

PERFORMANCE PLOT

WM8956-6158-FL32-M-REV1 -- Analogue BypassTHD+N v Amplitude (L/RINPUT3, HPL/R)
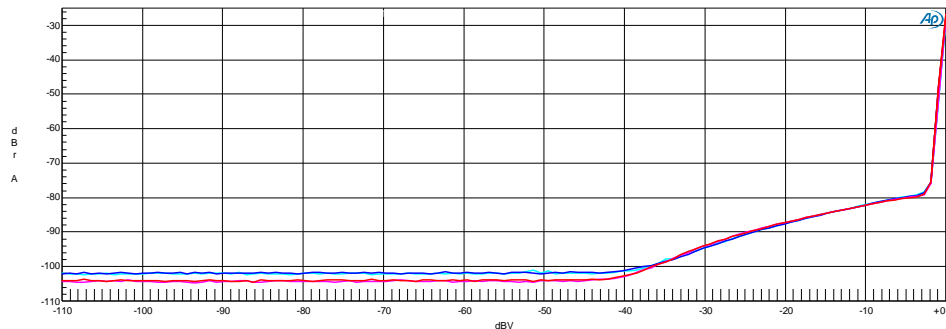
| Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	2	Anlr.THD+N Ampl	Left	HPL (16R)
1	2	Blue	Solid	2	Anlr.THD+N Ampl	Left	HPR (16R)
2	1	Magenta	Solid	2	Anlr.THD+N Ampl	Left	HPL (16R) A-weight
2	2	Red	Solid	2	Anlr.THD+N Ampl	Left	HPR (16R) A-weight

System AP2
Board: WM8956-6158-FL32-M-REV1-S
Device Date Code: 79AADUT
Input Signal: 997Hz; 0dBV;
Reference Levels: 0dBrA = -1.288 dBV
Supplies: AVDD=DCVDD=DBVDD = +3.3V
Input Signal Path: L/RINPUT3
Output Signal Path: HPL/R (16R Load)
BW Filtering: 22Hz-20kHz
Additional Filtering Type: As stated
Dither = Off
RMS or Averaging = Average
Load = 16R
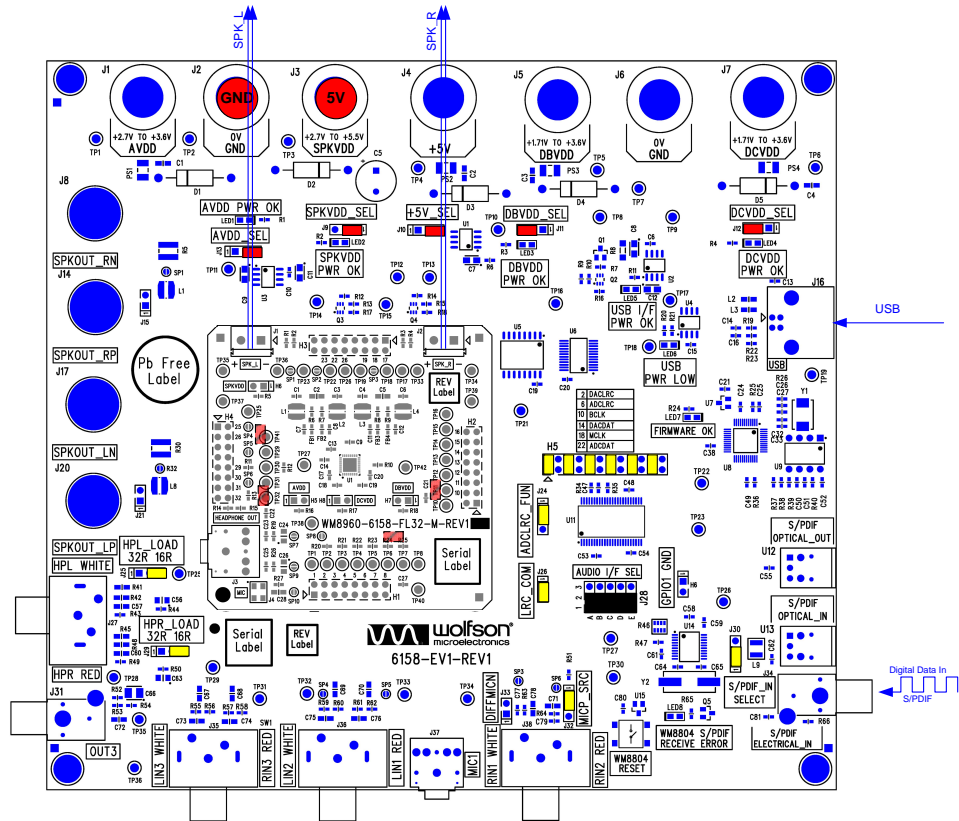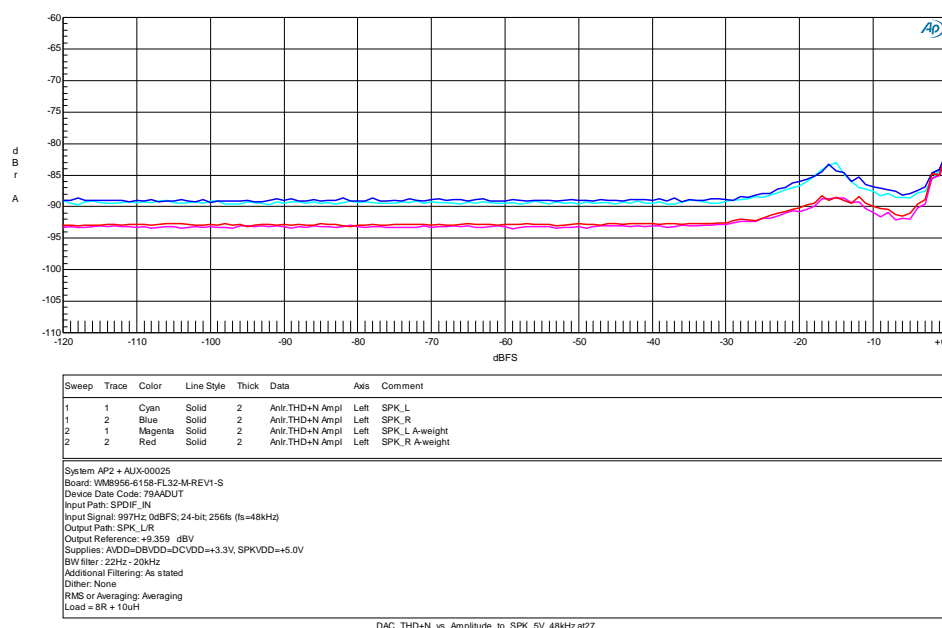
THD+N_vs_Amplitude_LRINPUT3_to_LROUT1_Bypass.at27

DAC PLAYBACK TO 8Ω SPEAKER (MINI BOARD)

The following section details board configuration for DAC playback to 8Ω speaker (Mini board).

BLOCK DIAGRAM
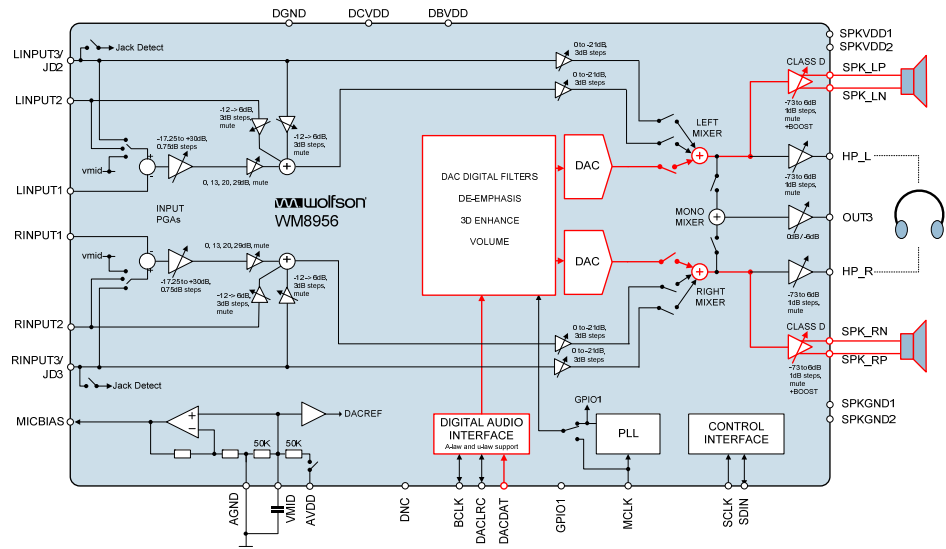
BOARD CONFIGURATION

= Jumper fitted on main board
(concealed by mini board)

REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

REG INDEX	DATA VALUE	COMMENT
R15	0x000	Reset
R25	0x0C0	VMID=50K, Enable VREF
R26	0x198	Enable DACL, DACR, SPKL and SPKR
R47	0x00C	Enable left output mixer and right output mixer
R49	0x0F7	Left and Right Speakers Enabled
R51	0x11B	DCGAIN = 1.52x (+3.6dB) and ACGAIN = 1.52x (+3.6dB)
R34	0x100	Left DAC to left output mixer enabled (LD2LO), 0dB
R37	0x100	Right DAC to right output mixer enabled (RD2RO), 0dB
R40	0x179	LSPK Vol = 0dB, volume update enabled
R41	0x179	RSPK Vol = 0dB, volume update enabled
R5	0x000	Unmute DAC digital soft mute

PERFORMANCE PLOT

WM8956-6158-FL32-M-REV1 -- DAC-SPK THD+N v Amplitude

Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	2	Anlr.THD+N Ampl	Left	SPK_L
1	2	Blue	Solid	2	Anlr.THD+N Ampl	Left	SPK_R
2	1	Magenta	Solid	2	Anlr.THD+N Ampl	Left	SPK_L A-weight
2	2	Red	Solid	2	Anlr.THD+N Ampl	Left	SPK_R A-weight

System AP2 + AUX-00025
Board: WM8956-6158-M-REV1-S
Device Date Code: 79AADUT
Input Path: SPDIF_IN
Input Signal: 997Hz; 0dBFS; 24-bit; 256fs (fs=48kHz)
Output Path: SPK_L/R
Output Reference: +9.359 dBV
Supplies: AVDD=DBVDD=DCVDD=+3.3V, SPKVDD=+5.0V
BW filter : 22Hz - 20kHz
Additional Filtering: As stated
Dither: None
RMS or Averaging: Averaging
Load = 8R + 10uH

DAC_THD+N_vs_Amplitude_to_SPK_5V_48kHz.at27

NOTES

1. The WM8956-6158-FL32_M_REV1 contains a low-pass filter on the bottom side of the PCB, which can be used to filter the Class D output signal for monitoring purposes. The filtered output can be observed on TP35/TP36 (left channel) and TP33/TP34 (right channel). When a suitable loudspeaker load is used, the on-board low-pass filter is not required. For efficiency and power consumption measurements of the class D output, it is recommended to remove R28/R29 (left channel) and R30/R31 (right channel) to avoid quiescent power consumption in the RC filter.

APPLICATION SUPPORT

If you require more information or require technical support, please contact the Wolfson Microelectronics Applications group through the following channels:

Email: apps@wolfsonmicro.com
Telephone Apps: +44 (0) 131 272 7070
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Mail: Applications Engineering at the address on the last page

or contact your local Wolfson representative.

Additional information may be made available on our web site at:

http://www.wolfsonmicro.com

IMPORTANT NOTICE

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