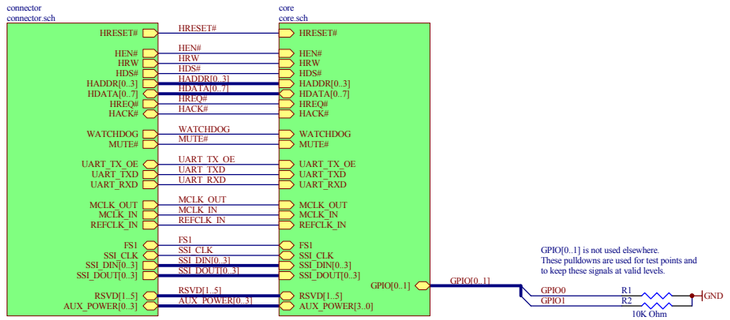
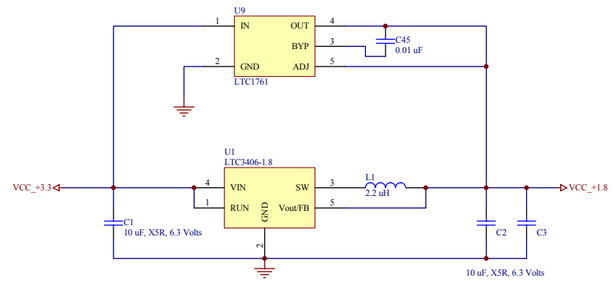


This linear regulator is used to assure that the +1.8v rail quickly passes the 0.5v threshold at powerup, thus minimizing power sequencing issues and making sure that the DSP does not draw excessive power as the power rails ramp up. This linear regulator is set with Vout=1.22v, so it is effectively shut off once the switching regulator comes up. Further testing and characterization of the DSP is require to determine if this linear regulator is in fact required.



This is a simple switching regulator. It produces 1.8V at >500 mA at about 90% efficency. A simple low drop out linear regulator would be a cheaper alternative at the expense of power. A linear regulator would dissapate about 0.75 watts max, This switching regulator dissapates about 0.10 watts max.

mech
mech.sch

Revision F

CIRRUS LOGIC®

CobraNet®

Cirrus Logic Confidential

Title: CM-2 Main Page

Cirrus Logic, Inc.
305 Interlocken Parkway
Broomfield, CO 80021
(303) 466-5228

Filename: cm2_main.sch
Sheet: 1 of 7
Date: 14-Jul-2005
PN: 600-00181-01

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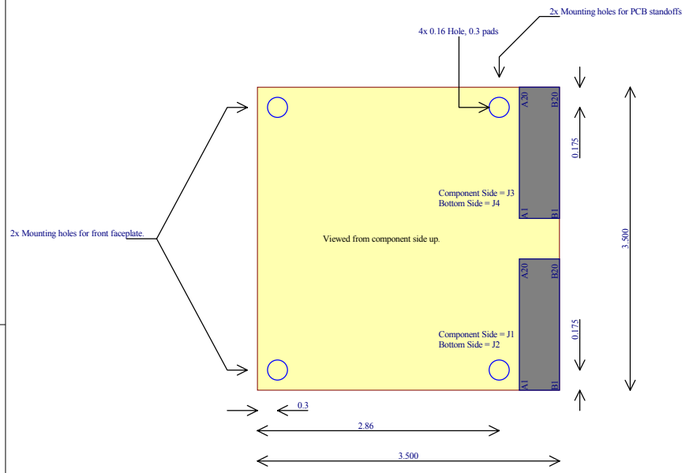
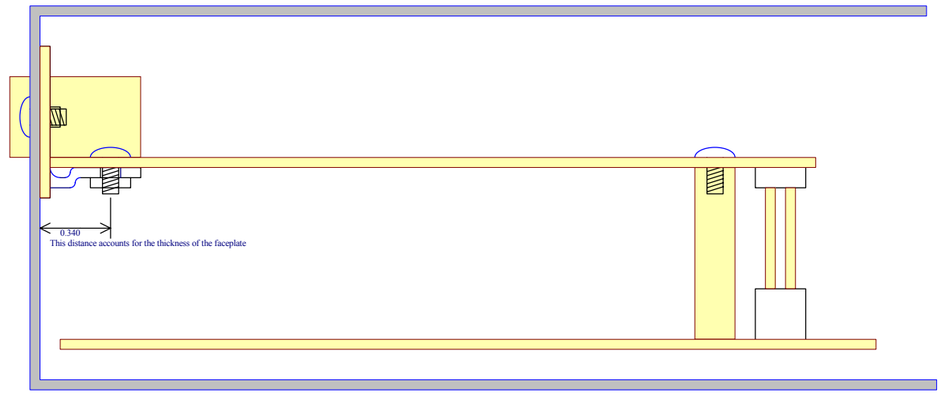
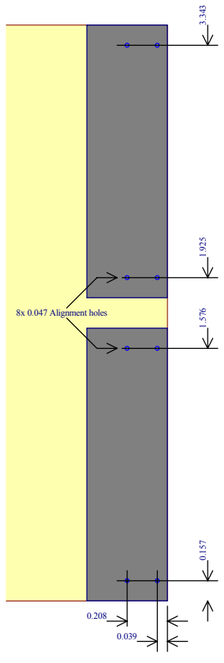


General PCB dimensions

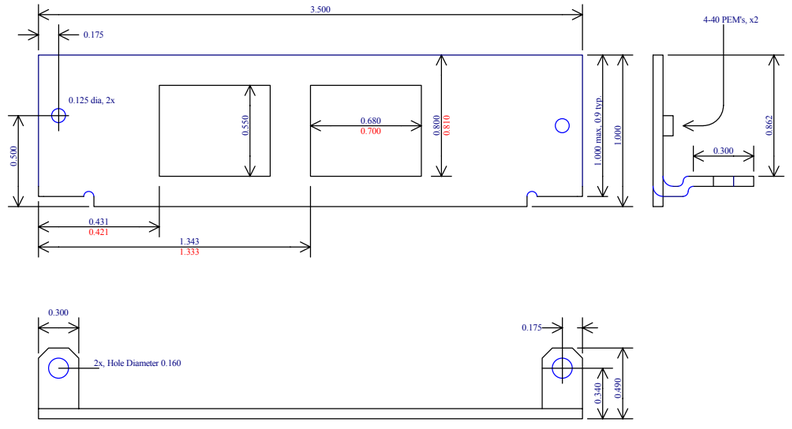


Example Configuration, Side View



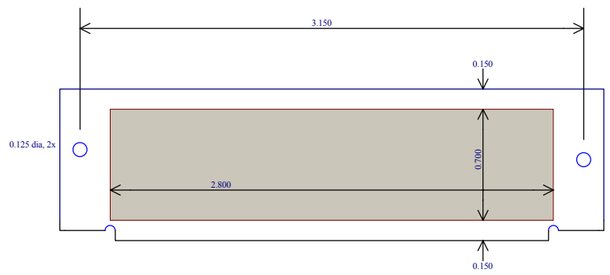
Connector Detail

Note: Mechanical dimensions for the CM-2 and CM-1 Rev F are identical. There are differences with earlier versions of the CM-1, however. For reference, earlier versions of the CM-1 dimensions are shown in RED.



Faceplate material is 20 guage, 0.037" thick, Cold Rolled Steel.
Plating is electroless nickel.

Faceplate Dimensions



Case cutout for faceplate mounting

Note: All dimensions are in inches.

Note: Drawing not to scale.

CobraNet®

Cirrus Logic, Inc.
305 Interlocken Parkway
Broomfield, CO 80021
(303) 466-5228

Title:

Filename: mech.sch
Sheet: 0 of 0
Date: 14-Jul-2005
PN: 600-00181-01

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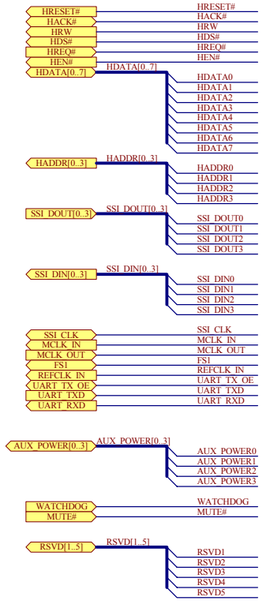
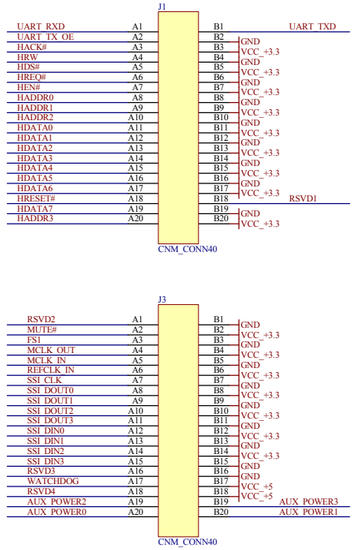
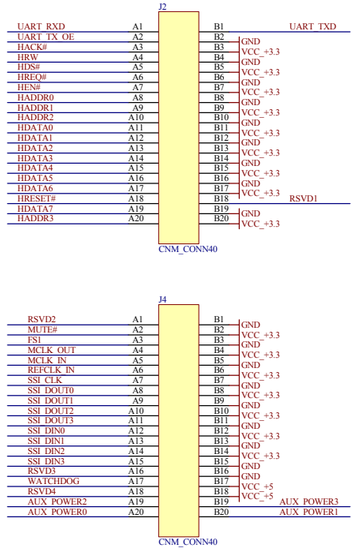
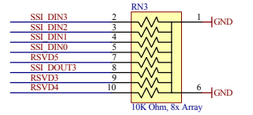
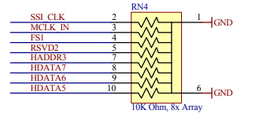


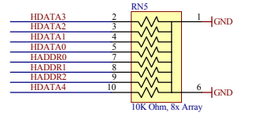


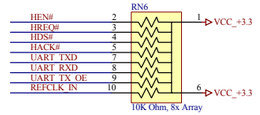


Note: Pull-ups/downs on SSI_DOUT[0..4] are located on the DSP schematic page.

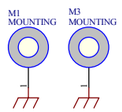




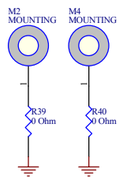




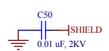
These pullups/downs are used to assure a valid logic level if a signal is tri-stated or not connected. In some situations, these may not be required.



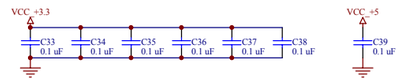
These two mounting holes are located near the front panel of the CM-2.



These two mounting holes are located at the "back" of the CM-2, near the main interface connectors.

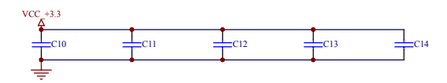


Place near the Ethernet connectors.



AC Signal Return Path Caps

Note: Similar AC signal return path caps must be included on the motherboard near the connector.



Power Decoupling Caps

CobraNet®

Cirrus Logic Confidential

Title: Host Interface Connector

Cirrus Logic, Inc.
305 Interlocken Parkway
Broomfield, CO 80021
(303) 466-5228

Filename: connector.sch
Sheet: 7 of 7
Date: 14-Jul-2005
PN: 600-00181-01

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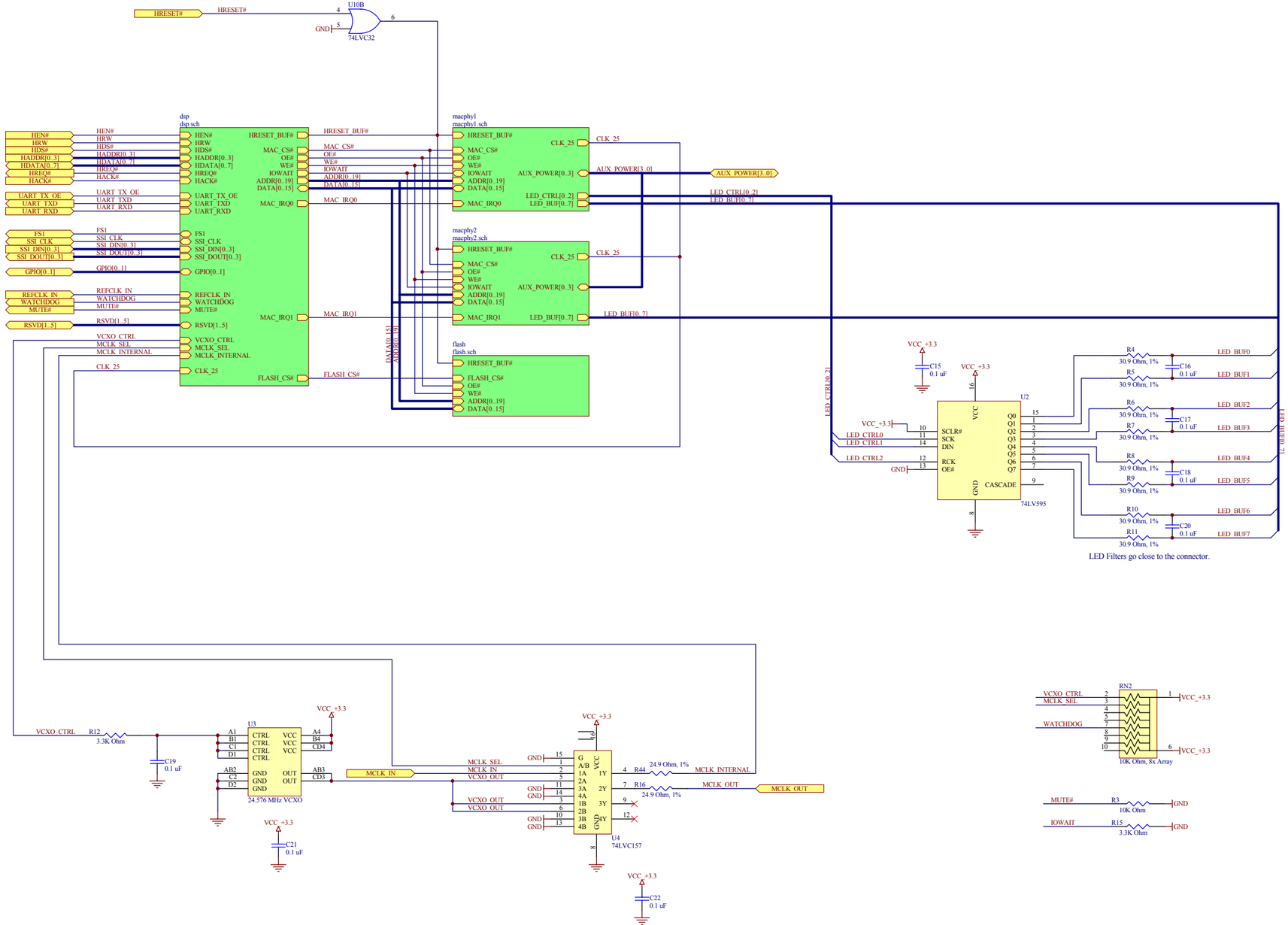
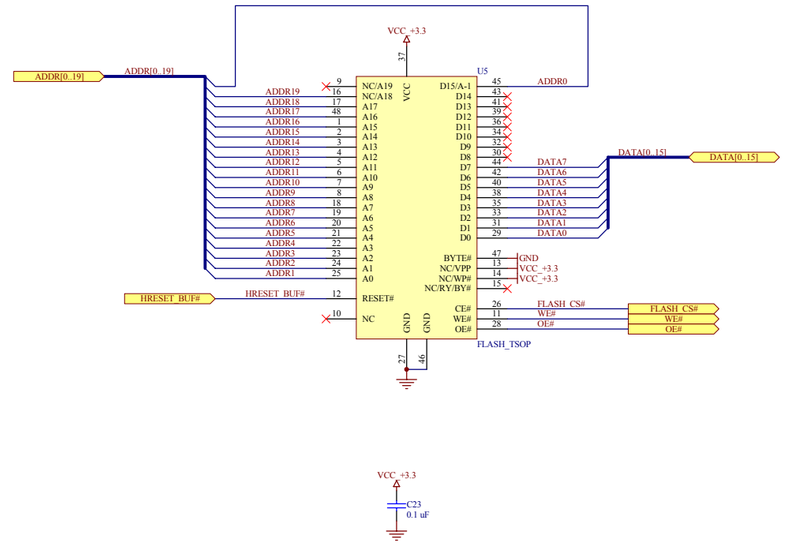


CobraNet

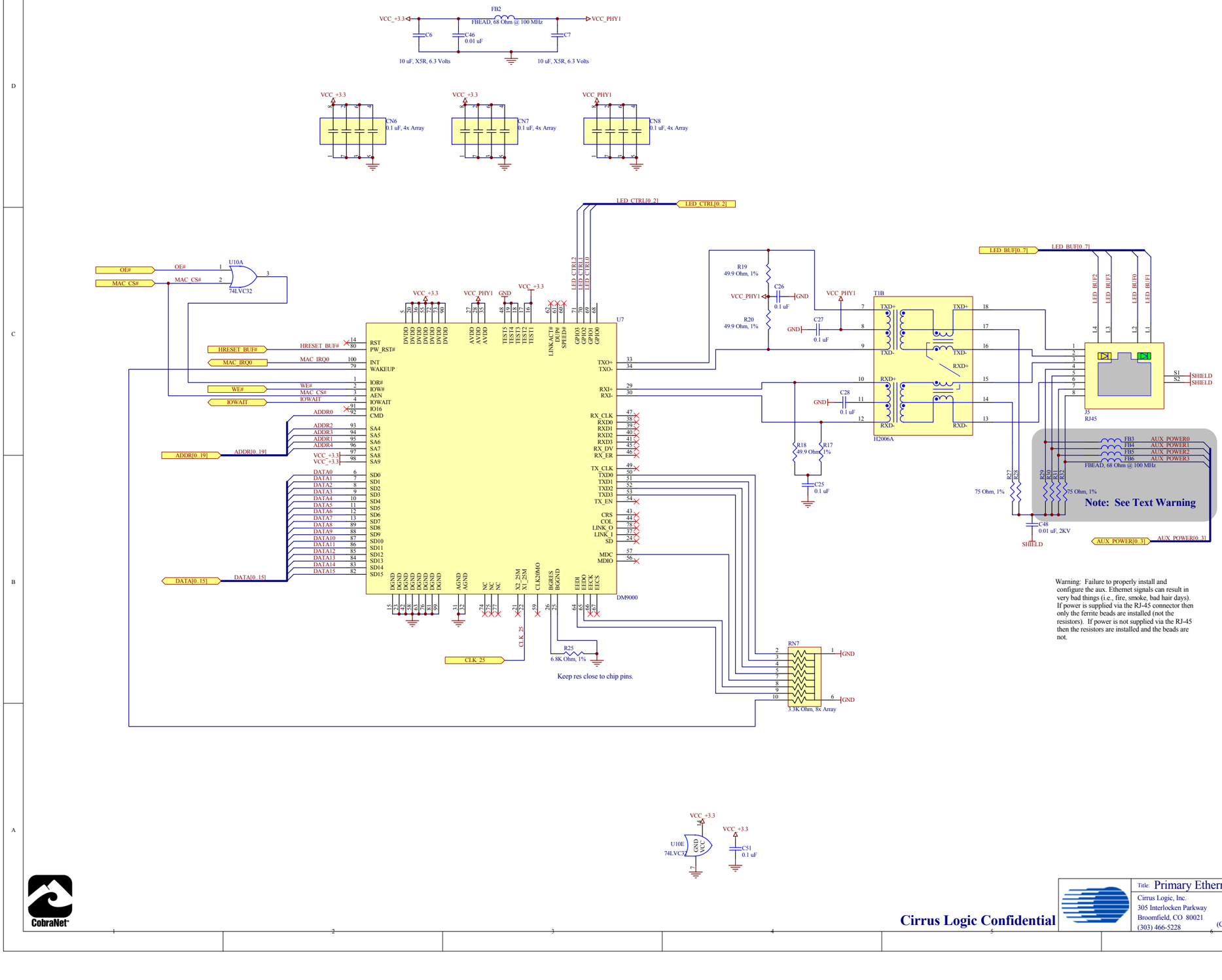
Cirrus Logic Confidential

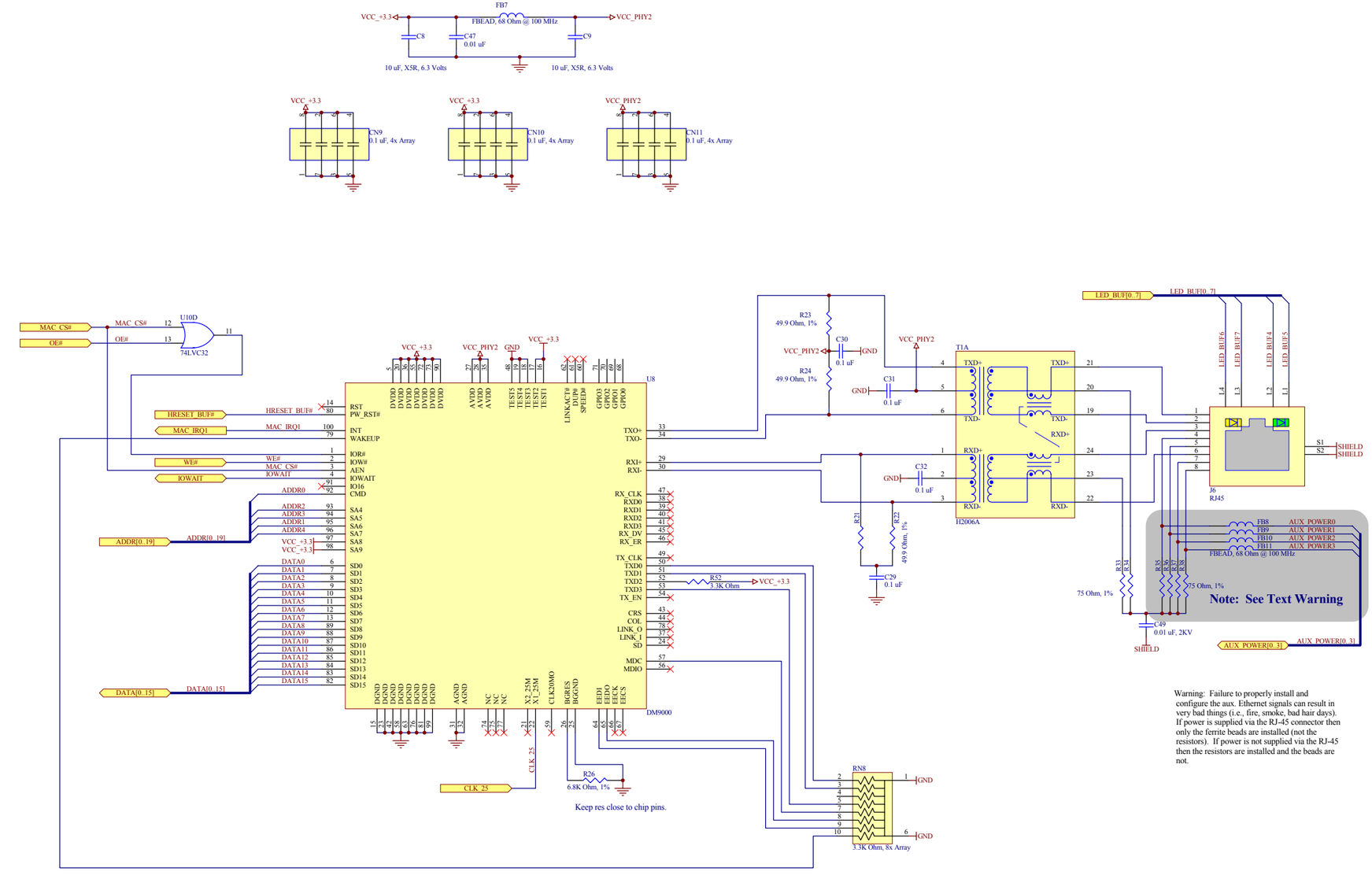
Title: Mamba Core	
Cirrus Logic, Inc. 305 Interlocken Parkway Broomfield, CO 80021 (303) 466-5228	Filename: core.sch Sheet: 2 of 7 Date: 14-Jul-2005 PN: 600-00181-01 (C) 2002, Cirrus Logic, Inc.



Cirrus Logic Confidential

Title:	Flash Memory
Cirrus Logic, Inc.	Filename: flash.sch
305 Interlocken Parkway	Sheet: 3 of 7
Broomfield, CO 80021	Date: 14-Jul-2005
(303) 466-5228	PN: 600-00181-01
	(C) 2002, Cirrus Logic, Inc.


FB2
FBEAD, 68 Ohm @ 100 MHz
VCC_+3.3
VCC_PHY1
C6
C46
0.01 uF
C7
10 uF, X5R, 6.3 Volts
10 uF, X5R, 6.3 Volts
CN6
0.1 uF, 4x Array
CN7
0.1 uF, 4x Array
CN8
0.1 uF, 4x Array
LED_CTRL[0..2]
U10A
74LVC32
OE#
MAC_CS#
HRESET_BUF#
MAC_IRQ0
WE#
IOWAIT
ADDR0
ADDR2
ADDR3
ADDR1
ADDR4
ADDR[0..19]
DATA[0..15]
U7
DM9000
RST
PW_RST#
INT
WAKEUP
IOR#
IOW#
AEN
IOWAIT
IO16
CMD
SA4
SA5
SA6
SA7
SA8
SA9
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
TXO+
TXO-
RXI+
RXI-
RX_CLK
RXD0
RXD1
RXD2
RXD3
RX_DV
RX_ER
TX_CLK
TXD0
TXD1
TXD2
TXD3
TX_EN
CRS
COL
LINK_O
LINK_I
SD
MDC
MDIO
CLK_25
R25
6.8K Ohm, 1%
Keep res close to chip pins.
RN7
3.3K Ohm, 8x Array
R19
49.9 Ohm, 1%
R20
49.9 Ohm, 1%
C26
0.1 uF
C27
0.1 uF
C28
0.1 uF
C25
0.1 uF
R18
49.9 Ohm, 1%
R17
1%
T1B
H2006A
TXD+
TXD-
RXD+
RXD-
LED_BUF[0..7]
J5
RJ45
S1
S2
SHIELD
FB3
FB4
FB5
FB6
AUX_POWER0
AUX_POWER1
AUX_POWER2
AUX_POWER3
FBEAD, 68 Ohm @ 100 MHz
R27
R28
R29
R40
R31
R32
75 Ohm, 1%
75 Ohm, 1%
Note: See Text Warning
C48
0.01 uF, 2KV
AUX_POWER[0..3]
Warning: Failure to properly install and configure the aux. Ethernet signals can result in very bad things (i.e., fire, smoke, bad hair days). If power is supplied via the RJ-45 connector then only the ferrite beads are installed (not the resistors). If power is not supplied via the RJ-45 then the resistors are installed and the beads are not.
U10E
74LVC32
C51
0.1 uF
CobraNet
Cirrus Logic Confidential
Title: Primary Ethernet
Cirrus Logic, Inc.
305 Interlocken Parkway
Broomfield, CO 80021
(303) 466-5228
Filename: macphy1.sch
Sheet: 5 of 7
Date: 14-Jul-2005
PN: 600-00181-01
(C) 2002, Cirrus Logic, Inc.


FB7
VCC_+3.3
FBEAD, 68 Ohm @ 100 MHz
VCC_PHY2
C8
10 uF, X5R, 6.3 Volts
C47
0.01 uF
C9
10 uF, X5R, 6.3 Volts
CN9
0.1 uF, 4x Array
CN10
0.1 uF, 4x Array
CN11
0.1 uF, 4x Array
U10D
74LVC32
MAC_CS#
OE#
U8
DM9000
HRESET_BUF#
MAC_IRQ1
WE#
IOWAIT
ADDR[0..19]
DATA[0..15]
CLK_25
R26
6.8K Ohm, 1%
Keep res close to chip pins.
R52
3.3K Ohm
R23
49.9 Ohm, 1%
R24
49.9 Ohm, 1%
C30
0.1 uF
C31
0.1 uF
C32
0.1 uF
C29
0.1 uF
R21
R22
49.9 Ohm, 1%
T1A
H2006A
LED_BUF[0..7]
J6
RJ45
S1
S2
SHIELD
FB8
FB9
FB10
FB11
AUX_POWER0
AUX_POWER1
AUX_POWER2
AUX_POWER3
FBEAD, 68 Ohm @ 100 MHz
R33
R34
75 Ohm, 1%
R35
R36
R37
R38
75 Ohm, 1%
Note: See Text Warning
C49
0.01 uF, 2KV
AUX_POWER[0..3]
RN8
3.3K Ohm, 8x Array
Warning: Failure to properly install and configure the aux. Ethernet signals can result in very bad things (i.e., fire, smoke, bad hair days). If power is supplied via the RJ-45 connector then only the ferrite beads are installed (not the resistors). If power is not supplied via the RJ-45 then the resistors are installed and the beads are not.
The secondary Ethernet MAC and connector are optional.
If it is not required then all parts on this page can be depopulated
(or removed entirely from a new design based on this circuit).
CobraNet
Cirrus Logic Confidential
Title: Secondary Ethernet
Cirrus Logic, Inc.
305 Interlocken Parkway
Broomfield, CO 80021
(303) 466-5228
Filename: macphy2.sch
Sheet: 6 of 7
Date: 14-Jul-2005
PN: 600-00181-01
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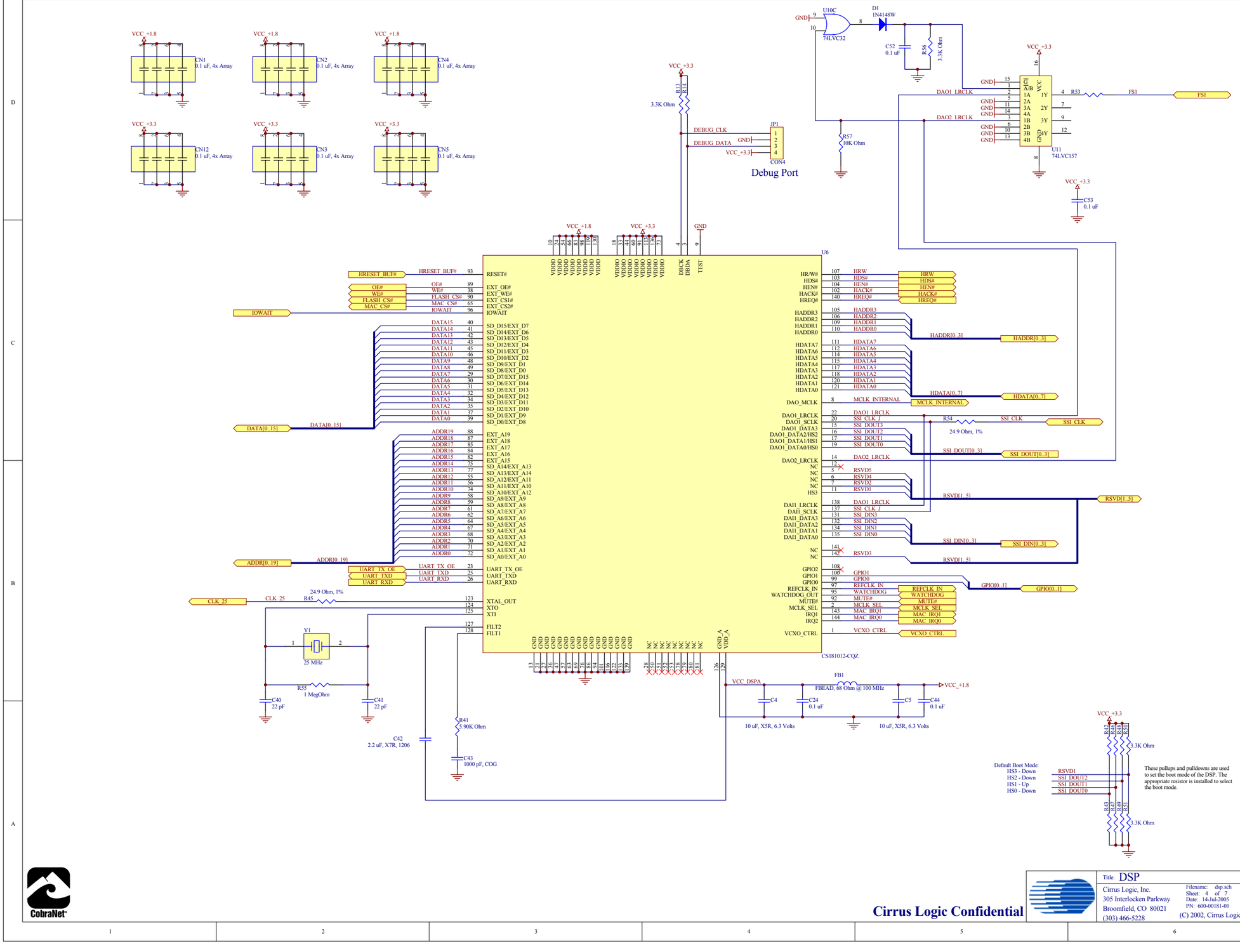
CN1 0.1 uF, 4x Array
CN2 0.1 uF, 4x Array
CN4 0.1 uF, 4x Array
CN12 0.1 uF, 4x Array
CN3 0.1 uF, 4x Array
CN5 0.1 uF, 4x Array
VCC_+1.8
VCC_+3.3
U10C
74LVC32
D1
1N4148W
C52
0.1 uF
R56
3.3K Ohm
R13
R14
3.3K Ohm
DEBUG_CLK
DEBUG_DATA
JP1
CON4
Debug Port
R57
10K Ohm
U11
74LVC157
DAO1_LRCLK
DAO2_LRCLK
R53
FS1
C53
0.1 uF
U6
CS181012-CQZ
RESET#
EXT_OE#
EXT_WE#
EXT_CS1#
EXT_CS2#
IOWAIT
SD_D15/EXT_D7
SD_D14/EXT_D6
SD_D13/EXT_D5
SD_D12/EXT_D4
SD_D11/EXT_D3
SD_D10/EXT_D2
SD_D9/EXT_D1
SD_D8/EXT_D0
SD_D7/EXT_D15
SD_D6/EXT_D14
SD_D5/EXT_D13
SD_D4/EXT_D12
SD_D3/EXT_D11
SD_D2/EXT_D10
SD_D1/EXT_D9
SD_D0/EXT_D8
EXT_A19
EXT_A18
EXT_A17
EXT_A16
EXT_A15
SD_A14/EXT_A13
SD_A13/EXT_A14
SD_A12/EXT_A11
SD_A11/EXT_A10
SD_A10/EXT_A12
SD_A9/EXT_A9
SD_A8/EXT_A8
SD_A7/EXT_A7
SD_A6/EXT_A6
SD_A5/EXT_A5
SD_A4/EXT_A4
SD_A3/EXT_A3
SD_A2/EXT_A2
SD_A1/EXT_A1
SD_A0/EXT_A0
UART_TX_OE
UART_TXD
UART_RXD
XTAL_OUT
XTO
XTI
FILT2
FILT1
DBCK
DBDA
TEST
HR/W#
HDS#
HEN#
HACK#
HREQ#
HADDR3
HADDR2
HADDR1
HADDR0
HDATA7
HDATA6
HDATA5
HDATA4
HDATA3
HDATA2
HDATA1
HDATA0
MCLK_INTERNAL
DAO_MCLK
DAO1_LRCLK
DAO1_SCLK
DAO1_DATA3
DAO1_DATA2/HS2
DAO1_DATA1/HS1
DAO1_DATA0/HS0
DAO2_LRCLK
NC
RSVD5
RSVD4
RSVD2
HS3
RSVD1
DAI1_LRCLK
DAI1_SCLK
DAI1_DATA3
DAI1_DATA2
DAI1_DATA1
DAI1_DATA0
GPIO2
GPIO1
GPIO0
REFCLK_IN
WATCHDOG_OUT
MUTE#
MCLK_SEL
IRQ1
IRQ2
VCXO_CTRL
HRW
HDS#
HEN#
HACK#
HREQ#
HADDR[0..3]
HDATA[0..7]
MCLK_INTERNAL
SSI_CLK_I
SSI_CLK
R54
24.9 Ohm, 1%
SSI_DOUT3
SSI_DOUT2
SSI_DOUT1
SSI_DOUT0
SSI_DOUT[0..3]
RSVD[1..5]
SSI_DIN3
SSI_DIN2
SSI_DIN1
SSI_DIN0
SSI_DIN[0..3]
GPIO1
GPIO0
GPIO[0..1]
REFCLK_IN
WATCHDOG
MUTE#
MCLK_SEL
MAC_IRQ1
MAC_IRQ0
VCXO_CTRL
HRESET_BUF#
OE#
WE#
FLASH_CS#
MAC_CS#
IOWAIT
DATA[0..15]
ADDR[0..19]
UART_TX_OE
UART_TXD
UART_RXD
CLK_25
24.9 Ohm, 1%
R45
Y1
25 MHz
R55
1 MegOhm
C40
22 pF
C41
22 pF
C42
2.2 uF, X7R, 1206
R41
5.90K Ohm
C43
1000 pF, COG
VCC_DSPA
FB1
FBEAD, 68 Ohm @ 100 MHz
C4
10 uF, X5R, 6.3 Volts
C24
0.1 uF
C5
10 uF, X5R, 6.3 Volts
C44
0.1 uF
R42
R44
R46
R50
R43
R47
R49
R51
3.3K Ohm
Default Boot Mode:
HS3 - Down
HS2 - Down
HS1 - Up
HS0 - Down
These pullups and pulldowns are used to set the boot mode of the DSP. The appropriate resistor is installed to select the boot mode.
CobraNet
Cirrus Logic Confidential
Title: DSP
Cirrus Logic, Inc.
305 Interlocken Parkway
Broomfield, CO 80021
(303) 466-5228
Filename: disp.sch
Sheet: 4 of 7
Date: 14-Jul-2005
PN: 600-00181-01
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