Technical Bulletin: CS5463
Functional & Performance Improvements in Revision D

Reference CS5463 Data Sheet revision DS678F2 dated April 2008.

Determining the Silicon Revision of the Integrated Circuit

On the front of the integrated circuit, directly under the part number, is an alpha-numeric line. Characters 3 and 4 in this line represent the silicon revision of the chip. For example, this line indicates that the chip is a "DX" revision chip:

NA**DX****YYWW

This Errata is applicable only to the D revision of the chip.

Dynamic Range of Pulse Outputs (E1, E2, E3)

Revision D

The dynamic range of the pulse outputs has been improved in rev D. When using the pulse outputs to measure energy accuracy, the device now meets all specified typical accuracy levels listed in the Characteristics and Specifications section of the data sheet.

Pulse Start-up Differences: E1 vs. E2 & E3

Revision C

In Revision C of the CS5463, when continuous conversions begin (except for the very first set of continuous conversions after reset) , the E1 pulse output start-up is not coincident with E2 & E3 start-up.

Revision D

This has been corrected.

Programmable Pulse Widths

Revision C

Revision C of the CS5463 had only one fixed pulse width.

Revision D

A register named *PulseWidth* (Page 1, Address 0) has been added that defines the width of pulse outputs in units of 1 OWR sample. The range is from 1 to 838607. The default value is 1 to be compatible with the earlier revisions.

$$T_{PW} = PulseWidth \times \frac{1}{(MCLK/K)/1024}$$

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Power Consumption

Revision C

Typical power consumption specification: I_{A+} = 1.3 mA

Revision D

Typical power consumption specification: I_{A+} = 1.1 mA

Temperature Sensor

Revision C

In revision C of the CS5463, the temperature sensor has a potential for failure in the low-temperature ranges. Additionally it showed linearity problems and chip-to-chip variations.

Revision D

In revision D of the CS5463, the temperature gain (T_{Gain}) and temperature offset (T_{Off}) register default values have been updated to the following values to improve the dynamic range and accuracy of the temperature sensor.

T_{Gain} (Page 1, Address 2) = 0x2F02C3

T_{Off} (Page 1, Address 3) = 0xF3D35A

IIR Filter Disable Bit

Revision C

In revision C of the CS5463 the IIR compensation filters enable bit ($\overline{IIR}$, Page 0, Address 18, Bit 4) could not be disabled.

Revision D

In revision D of the CS5463 this problem has been corrected.

$\overline{IIR}$ = 0 = IIR Compensation Filters Enabled (default)

$\overline{IIR}$ = 1 = IIR Compensation Filters Disabled

No Load Threshold

Revision C

Revision C of the CS5463 does not have a way to set the no load threshold.

Revision D

Revision D of the CS5463 has been modified to include the $LOAD_{Min}$ register (Page 1, Address 1). Use this register to set the no load threshold.

When the magnitude of the P_{active} register is less than $LOAD_{Min}$, the active energy pulse output will be disabled.

$LOAD_{Min}$ is a two's complement value in the range of $-1.0 \leq value < 1.0$, with the binary point to the right of the MSB. Negative values are not allowed.

High-pass Filter (HPF) Settling Time and AFC Function

Revision D

In revision D of the CS5463, HPF settling time is increased to 3000/OWR seconds in order to remove possible, initial fault pulses on E1, E2, and E3 outputs.

Be aware that when using the automatic line frequency calculation (AFC) function with any HPF enabled, the AFC should be enabled at least 3000/OWR seconds after the continuous conversions begin. Failing to do so will cause unstable and inaccurate Epsilon and Q_{AVG} results during the first 20 seconds of conversions (50 Hz line frequency).

DRDY (Data Ready) Delay After Conversion Start

Revision C

The DRDY bit in the Status register is set T seconds after the start of the conversion, where T equals:

$$T = N \times \frac{1}{(MCLK/K)/1024}$$

N equals the value loaded in the Cycle Count register.

Revision D

In revision D of the CS5463, the delay is increased by 3000 cycles or 750 ms (OWR = 4000) if any HPF is enabled. Or the time between the start of a conversion and the setting of the DRDY bit is T seconds if any HPF is enabled, where T equals:

$$T = N \times \frac{1}{(MCLK/K)/1024} + \frac{3000}{(MCLK/K)/1024}$$

N equals the value loaded in the Cycle Count register.

AC Offset Calibration

Revision C

In revision C of the CS5463, AC offset calibration would result in the I_{ACOFF} and V_{ACOFF} values being twice as large as necessary.

Revision D

In revision D of the CS5463, this problem has been corrected.