CDB4244

CS4244 Evaluation Board

Features

♦ Multiple Analog Input Filter Options
  – Active Single Ended to Differential
  – Passive Differential

♦ Multiple Analog Output Filter Options
  – Passive Single Ended & Differential
  – Active Single Ended & Differential
  – Active Differential to Single Ended

♦ Versatile S/PDIF Interface
  – CS8416 Digital Audio Receiver
  – CS8406 Digital Audio Transmitter
  – CS2000 Clock Synthesizer

♦ External Connection Headers
  – Control Port Accessibility
  – DSP Serial Audio I/O Accessibility

♦ Windows® Compatible FlexGUI S/W Control
  – Allows Easy Configuration of the CDB4244
  – Predefined & User-Configurable Scripts

Description

The CDB4244 evaluation board is an excellent platform designed to facilitate evaluation of the CS4244 multi-channel CODEC. Use of the board requires an analog/digital signal source, an audio analyzer, and power supplies. A Windows PC-compatible computer is also needed in order to configure the board.

System timing for the I²S and Left-Justified serial interface formats can be accomplished using S/PDIF I/O or crystal-based timing hardware on the CDB4244. An external DSP interface header supports I²S, Left-Justified, and TDM serial interface formats.
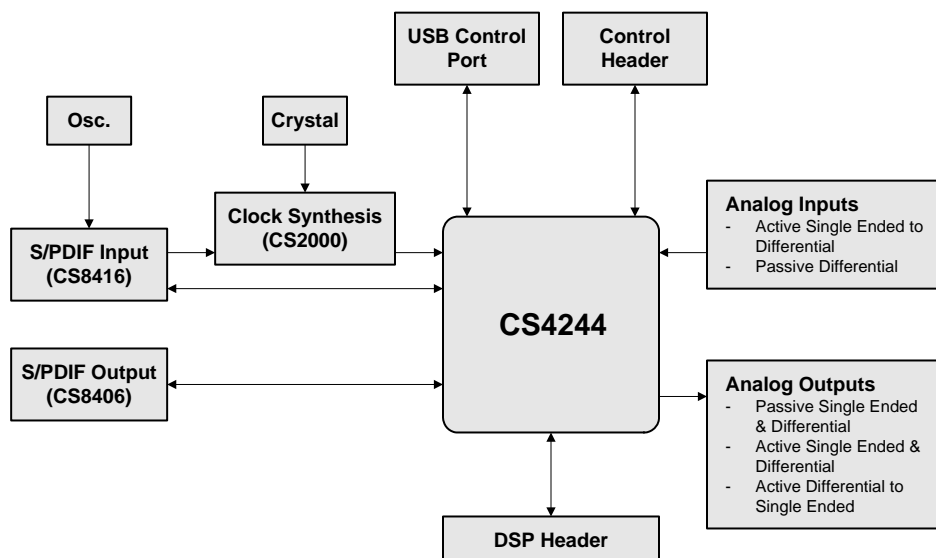
1/8" audio jacks, three-pin headers, and RCA phono jacks are provided for the CS4244 analog I/O connections. Digital I/O connections are accomplished through RCA phono jacks or optical connectors leading to the S/PDIF receiver and transmitter.

The Windows-based software available online makes configuring the CDB4244 easy. The software communicates through the PC's USB port to control the CS4244, the S/PDIF receiver and transmitter, and the clock synthesizer. These devices can also be controlled through an external control header for easy in-system evaluation.

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1 SYSTEM OVERVIEW

The CDB4244 platform provides analog and digital interfaces to the CS4244 and allows for external DSP and I²C^{TM} control. Board configuration can be done using the Windows PC-compatible graphical user interface (GUI) to read and write device registers. Multiple analog input and output filter configurations are supported, as well are several different options for generating a system master clock.

The CDB4244 schematic set has been partitioned into eight pages and is shown in Section 8 starting on page 23. Additionally, Section 6 on page 20 provides a description of all external connectors, including the default factory settings for all jumpers.

1.1 Power

Power is supplied to the board through an external regulated +5-V supply or a PC USB port. The CS4244 analog supply (referred to as VA) may be taken from the selected +5-V supply or an onboard +3.3-V regulator. Table 4 on page 21 explains how to configure each option. A dual-rail ±12-V regulated supply is required to power the active filter network used for each analog input channel. A special resistor option allows the optional active analog output filter configurations to use either a single-rail or dual-rail power supply.

Shunt jumpers and 1%, 1-Ω parallel resistors provide a convenient way to measure both the VA and VL supply currents to the CS4244. The current is easily calculated by measuring the voltage drop across each resistor with its associated shunt removed. The shunts connected in parallel with these resistors must be in place during normal operation.

WARNING: Please refer to the CS4244 data sheet for allowable voltage levels.

1.2 Grounding and Power Supply Decoupling

The CS4244 requires careful attention to power supply and grounding arrangements to optimize performance. The CDB4244 demonstrates these optimal arrangements. Figure 18 on page 31 shows the component placement; Figure 19 on page 32 shows the top-side layout and Figure 22 on page 35 shows the bottom-side layout. Power supply decoupling capacitors are located as close as possible to the CS4244. Extensive use of ground plane fill helps reduce radiated noise.

1.3 CS4244 Multi-Channel CODEC

A complete description of the CS4244 (Figure 10 on page 23) can be found in the CS4244 data sheet. The CS4244 is configured using the Cirrus Logic FlexGUI software. The device configuration registers are accessible via the "Register Maps" tab of the software. This tab provides low-level control of each bit in the device's control port. The "CODEC Control" and "Volume Control" tabs provide high-level control of the device for faster configuration. See Section 2 on page 7 for details.

1.4 CS8406 Digital Audio Transmitter

The CS8406 S/PDIF transmitter (Figure 11 on page 24) converts the digital audio generated by the CS4244 (I²S or Left-Justified serial interface formats) to the standard S/PDIF data stream and routes these signals to the optical and RCA connectors on the CDB4244. With a supplied master clock, the CS8406 can master the serial audio interface timing for the CDB4244.

The CS8406 can be controlled using the Cirrus Logic FlexGUI software under the "Board Control" tab. See Section 2.1 on page 8 for details. A complete description of the CS8406 and a discussion of the digital audio interface can be found in the CS8406 data sheet.

1.5 CS8416 Digital Audio Receiver

The CS8416 S/PDIF receiver (Figure 11 on page 24) converts the incoming S/PDIF data stream from the optical or RCA connectors into digital audio (I²S or Left-Justified serial interface formats) and passes it to the CS4244. Using the master clock recovered from the incoming S/PDIF stream or the clock provided by the socketed onboard oscillator, the CS8416 can master the serial audio interface timing for the CDB4244.

The CS8416 can be controlled using the Cirrus Logic FlexGUI software under the "Board Control" tab. See Section 2.1 on page 8 for details. A complete description of the CS8416 and a discussion of the digital audio interface can be found in the CS8416 data sheet.

1.6 CS2000 Fractional-N Clock Synthesizer & Clock Multiplier

The CS2000 clock synthesizer (Figure 11 on page 24) provides a low-jitter master clock source for the CS4244 and CS8406, and is capable of generating the necessary master clock frequencies to provide multiple sample rates without having to make hardware changes to the board. The Cirrus Logic FlexGUI software can be used to easily realize many of the clocking options available for the CDB4244.

Refer to Section 3 on page 13 for a detailed explanation of how the CS2000 can be used with the CDB4244. A complete description of the CS2000 can be found in the CS2000 data sheet.

1.7 Oscillator

The socketed onboard oscillator (Figure 11 on page 24) can serve as the master clock for the CDB4244 when the CS8416 can no longer recover a master clock from the incoming S/PDIF stream. Refer to Section 3.1 on page 13 for more information. The oscillator is mounted in pin sockets, allowing easy removal or replacement. The CDB4244 can accommodate +5-V half-can oscillators.

1.8 External Connection Headers

The CDB4244 has been designed to allow connections to and from an external system through a DSP header (J2 in Figure 10 on page 23) and a control port header (J1 in Figure 10 on page 23). The DSP header provides access to the serial audio signals required to interface with an external system. The control port header provides bidirectional access to the I²C control port signals. Two unpopulated pull-up resistors (R165 and R166) are also available in the event that the external host does not have pull-up resistors on its I²C lines.

These headers are accessed by removing the jumpers from the "Jumper for Bd Control" position labeled on the board. The user may then connect a ribbon cable connector to the "Ext Control Connection" pins for external control of the CDB4244. A single row of "GND" pins are provided to maintain signal ground integrity. If the headers are not in use, the jumpers must be in place for each row of J1 and J2 in the "Jumper for Bd Control" position. In this configuration, the CDB4244 assumes full control of the CS4244, with access through the PC USB connection.

Note that the CS4244 $\overline{INT}$ pin defaults to an active-low, open-drain interrupt output. The CDB4244 does not have a pull-up resistor to pull the interrupt signal high once it is deasserted by the CS4244. Instead, the interrupt signal is pulled high by a pull-up resistor internal to the onboard microcontroller. If the CDB4244 is controlled externally (through the use of J1), the external system must be able to pull the interrupt signal high if the CS4244 $\overline{INT}$ pin remains in its default open-drain configuration. Alternatively, the $\overline{INT}$ pin may be configured as active high or active low, avoiding the need for a pull-up resistor in this case. Refer to the CS4244 data sheet for more information.

To pass digital audio data from the ADCs of the CS4244 directly to the DACs in order to evaluate analog-in-to-analog-out performance, remove the jumpers from the SDOUT1, SDIN1, SDOUT2, and SDIN2 rows of the DSP header (J2). Then jumper SDOUT1 to SDIN1, and SDOUT2 to SDIN2 using the middle column of the DSP header.

1.9   Analog Inputs

The CDB4244 can accept single-ended analog input signals through the RCA phono jacks on each channel. An active single-ended-to-differential input filter network converts the single-ended input into a differential signal before the signal is passed to the respective differential analog inputs of the CS4244.

Space for a passive differential filter option allows differential analog input signals to be connected directly to the CDB4244. Stereo 1/8" audio jacks are provided to support this option; however, the components used to populate this filter option must be obtained separately. With either filter option, analog input signals are AC-coupled to the CS4244.

Refer to Section 4 starting on page 15 for details on the implementation of either input filter.

1.10   Analog Outputs

The CDB4244 provides differential analog outputs through the stereo 1/8" audio jacks on each output channel. While a passive filter network is populated on each output channel by default, each channel has space for an optional active differential filter network.

Both the active and passive differential filter options can be converted to provide single-ended outputs by removing certain components from the board. A fifth filter option provides space for an active differential-to-single-ended filter, which can convert the differential analog outputs of the CS4244 into a single-ended signal. RCA phono jacks are provided to support these options. The components used to populate any of the three active output filter options available for each channel must be obtained separately.

Refer to Section 5 starting on page 17 for details on the implementation of each output filter.

2 SOFTWARE MODE CONTROL

The CDB4244 can be used with the Microsoft Windows®–based FlexGUI graphical user interface, allowing software control of the CS4244, CS8416, CS8406, and CS2000 registers. The latest control software can be downloaded from www.cirrus.com/msasoftware. Step-by-step instructions for setting up the FlexGUI with the CDB4244 configured under the factory default settings are provided as follows:

1. Download and install the FlexGUI software as instructed on the Cirrus Logic website.
2. Connect a triple-output power supply to the binding posts marked "+5 V EXT, GND, -12 V, and +12 V."
3. Connect the CDB4244 to the host PC using a USB cable.
4. Launch the Cirrus Logic FlexGUI. *Once the GUI is launched successfully, all CS4244 registers are set to their default reset state, with the remaining devices preconfigured as necessary.*
5. Refresh the GUI by clicking on the "Update" button. *The state of all registers is now visible.*

For standard setup:

1. Set up the board's clocking and data options in the "Board Control" tab as desired.
2. Set up the CS4244 in the "CODEC Control" and "Volume Control" tabs as desired.
3. Begin evaluating the CS4244.

For quick setup, the CDB4244 may, alternatively, be configured by loading a predefined sample script file:
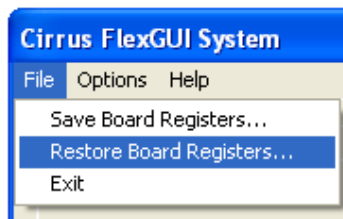
1. On the File menu, click "Restore Board Registers..."
2. Browse to the "Boards\CDB4244\Scripts" directory.
3. Choose any one of the provided scripts to begin evaluation.

To create custom script files:

1. On the File menu, click "Save Board Registers..."
2. Enter any name that sufficiently describes the current setup.
3. Choose the desired location, and save the script.
4. To load this script at a later time, follow the instructions above for loading a predefined sample script.
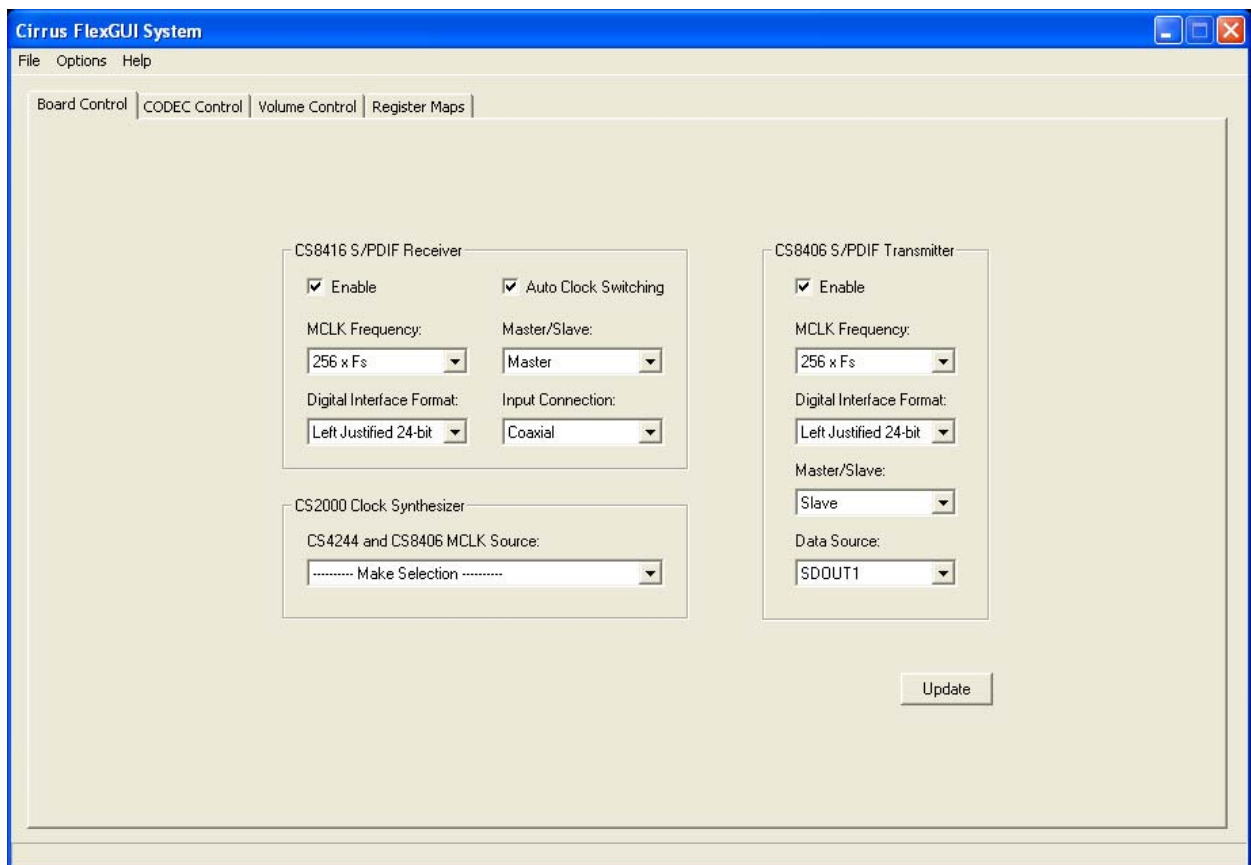
2.1   Board Control Tab

The "Board Control" tab provides high-level control of the clocking and data options within the CDB4244. A description of each control group is outlined below.

CS8416 S/PDIF Receiver—Configures the serial interface format of the S/PDIF receiver and indicates how the receiver is connected to the external transmitter (coaxial or optical).

CS8406 S/PDIF Transmitter—Configures the serial interface format of the S/PDIF transmitter and selects which data channel is passed to the outgoing S/PDIF stream: SDOUT1 (ADC1 and ADC2) or SDOUT2 (ADC3 and ADC4).

CS2000 Clock Synthesizer—Selects the master clock that is presented to the CS4244 and CS8406. Refer to Section 3 on page 13 for more information.

Update—Reads the registers of each device within the CDB4244 and reflects the current values in the GUI.

Figure 1. Board Control Tab

Note: Refer to the CS4244 data sheet for information on how to configure the device's clocking options in order to satisfy the device's recommended power up and power down sequence.

2.2 CODEC Control Tab

The "CODEC Control" tab provides high-level control of many CS4244 register settings. Status text detailing the CODEC's specific configuration is shown as part of certain controls. The text shown depends on the setting of the associated control. Note that the Update button (described below) must be pressed to show the current status of the CS4244 registers represented in this tab. A description of each control group is outlined below. See the CS4244 data sheet for complete register descriptions.

Serial Port Configuration—Configures the CS4244's serial port and provides controls for related interrupts. Note that changes to these settings during normal operation may violate the device's recommended power up or power down sequence; refer to the CS4244 data sheet for more information.

Power—Provides a means to power up or power down each ADC and DAC of the CS4244. Note that it is the user's responsibility to ensure that the "VA Selection" control correctly reflects the VA supply level.

Miscellaneous Controls—Configures interrupt behavior and various ADC options, as well as selects the CS4244's I²C address.

TDM Options—Configures the CS4244's serial port when operating in the TDM interface format. Note that the CS4244 cannot operate in TDM mode using the CDB4244 alone; instead the CS4244 must be controlled externally to exercise the device's TDM capabilities. Refer to Section 1.8 on page 5 for more information on how to release the CS4244 from the board's command and control it with an external device.

Update—Reads all registers in the CS4244 and reflects the current values in the GUI.

Reset—Resets the CS4244.
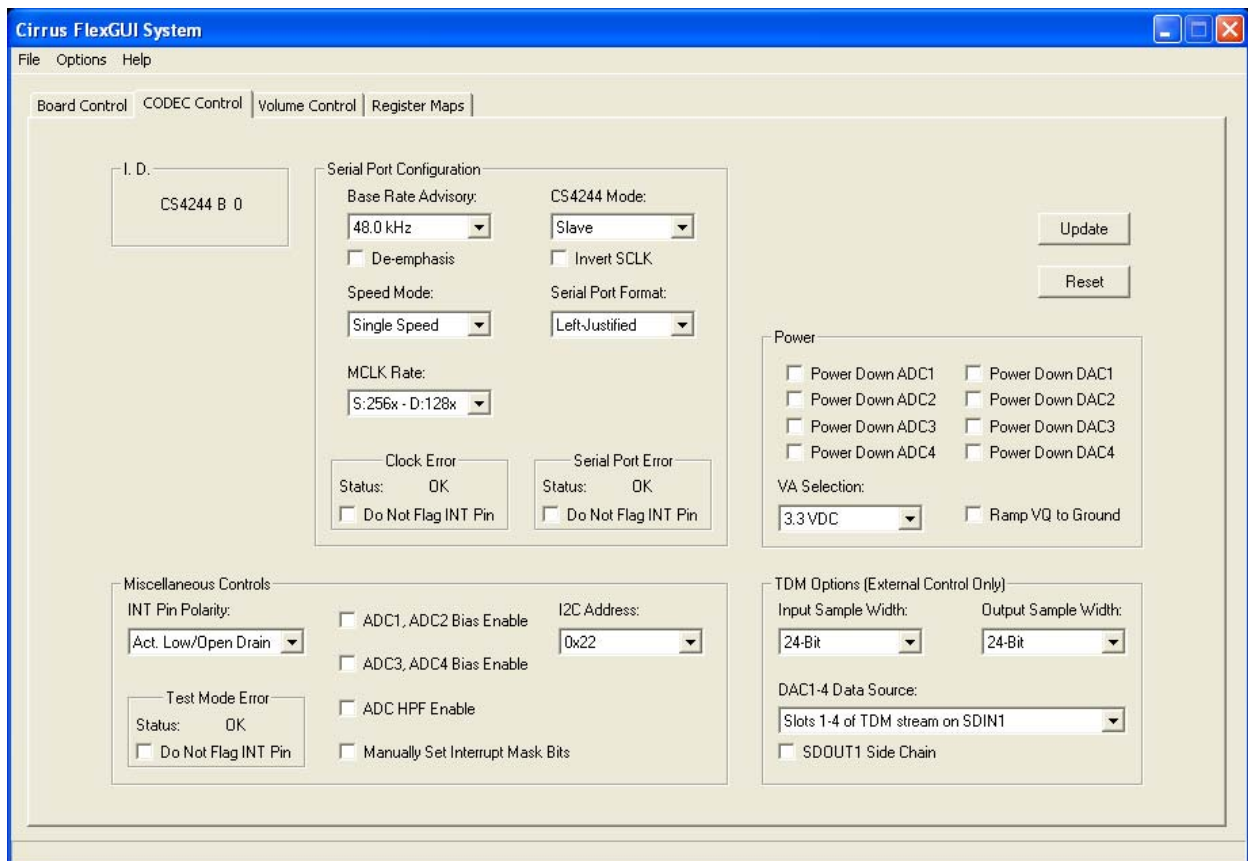
Figure 2. CODEC Control Tab
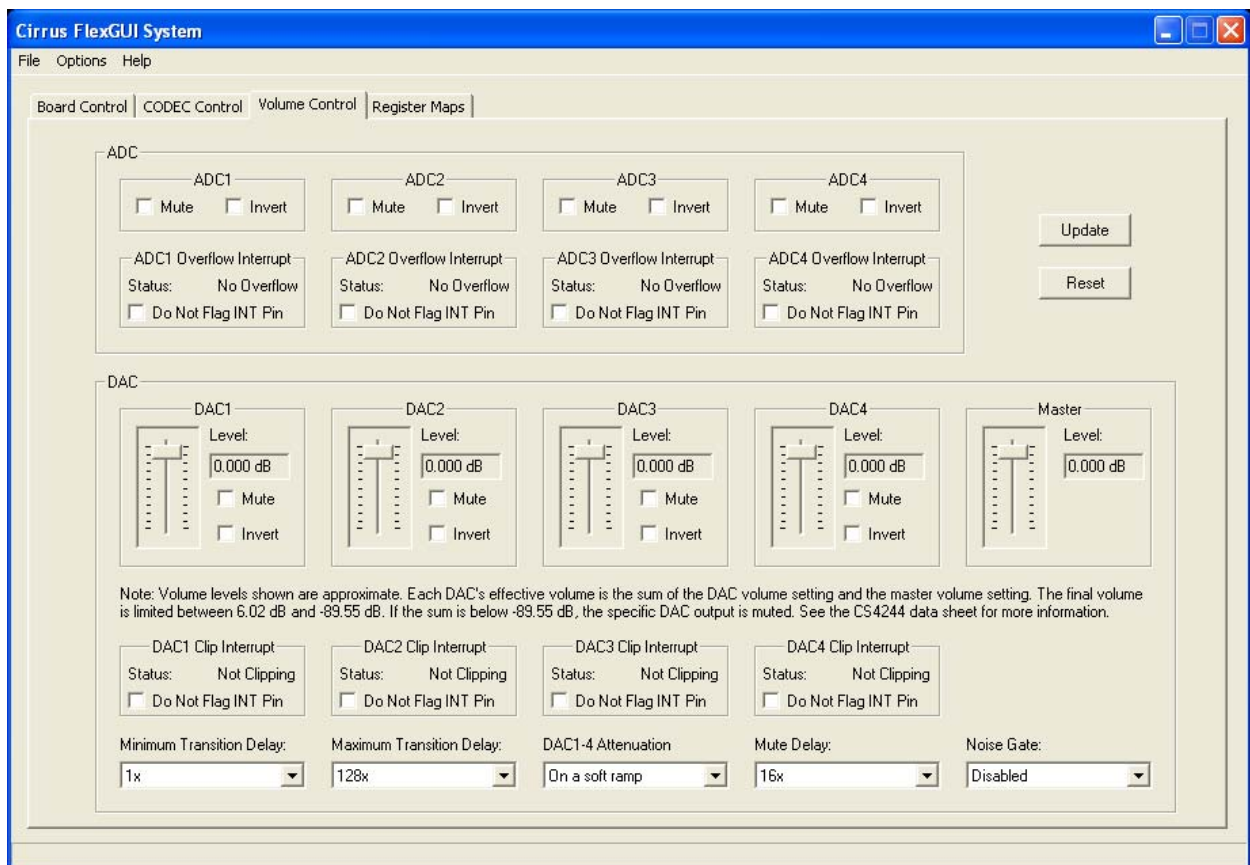
2.3 Volume Control Tab

The "Volume Control" tab provides high-level control of all volume-related settings for each ADC and DAC of the CS4244. Status text detailing the CODEC's specific configuration is shown as part of certain controls. The text shown depends on the setting of the associated control. Note that the Update button (described below) must be pressed to show the current status of the CS4244 registers represented in this tab. A description of each control group is outlined below. See the CS4244 data sheet for complete register descriptions.

ADC—Provides controls to mute or invert the output of each ADC and to control ADC overflow interrupts.

DAC—Provides volume, muting, and inversion controls for each DAC, as well as a master volume control. Fine volume control can be performed by clicking on the associated volume slider and using the arrow keys. This group also controls DAC volume changes, as well as DAC clipping interrupts.

*Update*—Reads all registers in the CS4244 and reflects the current values in the GUI.

Reset—Resets the CS4244.

Figure 3. Volume Control Tab

2.4 Register Maps Tab

The "Register Maps" tab provides low-level control over the register-level settings of the CS4244, CS8416, CS8406, CS2000, and microcontroller GPIO. Each device is displayed on a separate tab. Register values can be modified bitwise or bytewise. For bitwise control, click the appropriate push button for the desired bit. For bytewise control, the desired hexadecimal value can be typed directly into the register address box within the register map.
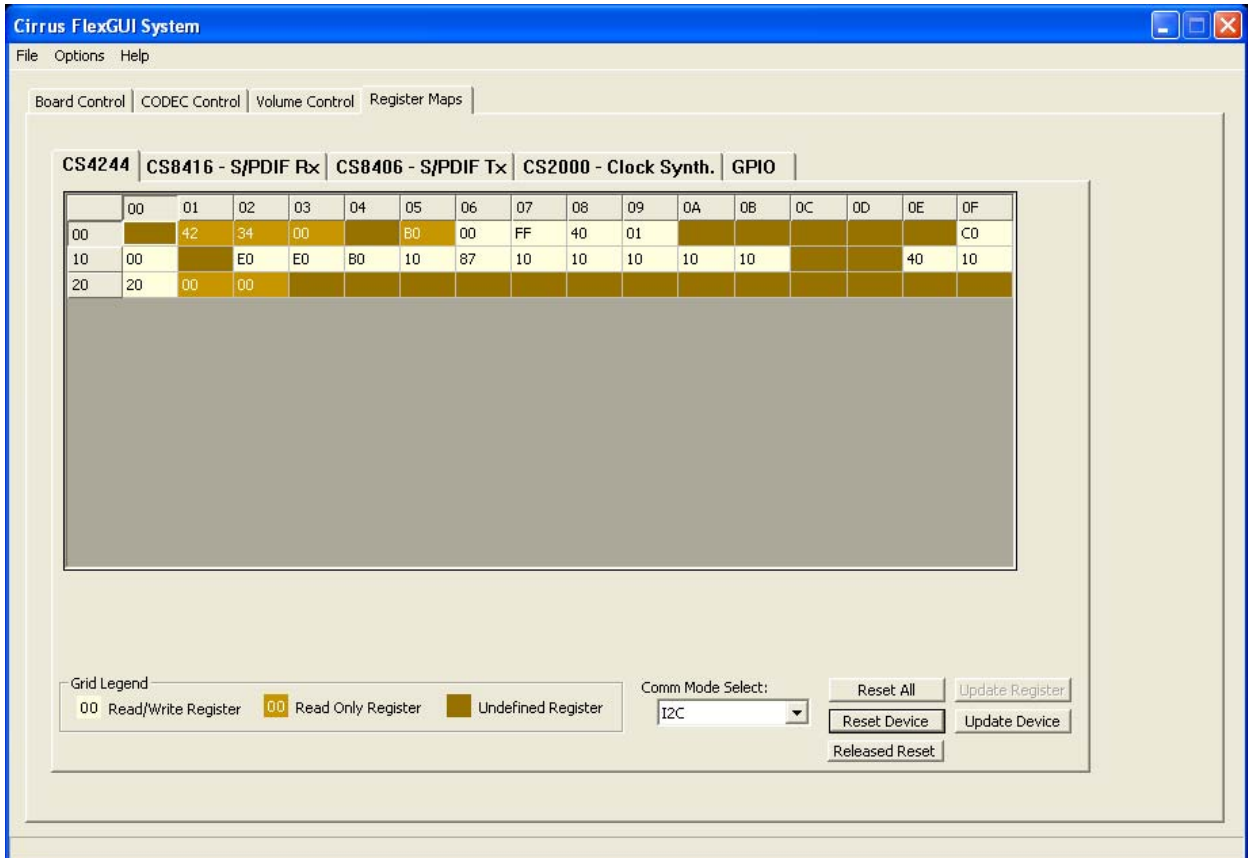
Figure 4. Register Maps Tab

Certain device tabs provide a means to reset the selected device through the use of the "Reset Device" button. The "Released Reset/Hold In Reset" button provides manual control of the selected device's reset pin, if applicable. The "Reset All" button resets the CDB4244.

The "Update Device" button reads all registers of the selected device and updates the register map accordingly. Highlighting a specific register and clicking the "Update Register" button reads only the selected register and refreshes its display in the register map.

2.5 Predefined Sample Scripts

The CDB4244 FlexGUI software comes furnished with four scripts that can quickly configure the board for use with an external S/PDIF transmitter and receiver. These scripts configure the CS4244, CS8416, and CS8406 to operate using the 24-bit Left-Justified serial interface format, with a master clock rate of 256 times the sample rate. The sample rate is set within the external S/PDIF source. System timing is mastered by the CS8416 at multiples of the sample rate set by the S/PDIF source.

The system master clock recovered by the CS8416 is passed through the CS2000 before being presented to the CS4244 and the CS8406. Serial audio data from the incoming S/PDIF stream is routed from the CS8416 to the SDIN1 and SDIN2 pins of the CS4244, while data on the SDOUT1 pin of the CS4244 is routed to the CS8406 to be sent along the outgoing S/PDIF stream. The CS4244 is configured to operate in single-speed mode; see the CS4244 data sheet for the range of allowable incoming sample rates. The four scripts are defined as follows:

QuickSetup_Coax_VA_3R3V_AIN12: Configures the CDB4244 as described above when an external S/PDIF transmitter is connected to the "S/PDIF IN" input of the board using a coaxial cable, and a 3.3-V supply is used to power VA.

QuickSetup_Coax_VA_5V_AIN12: Configures the CDB4244 as described above when an external S/PDIF transmitter is connected to the "S/PDIF IN" input of the board using a coaxial cable, and a 5-V supply is used to power VA.

QuickSetup_Optical_VA_3R3V_AIN12: Configures the CDB4244 as described above when an external S/PDIF transmitter is connected to the "S/PDIF IN" input of the board using an optical cable, and a 3.3-V supply is used to power VA.

QuickSetup_Optical_VA_5V_AIN12: Configures the CDB4244 as described above when an external S/PDIF transmitter is connected to the "S/PDIF IN" input of the board using an optical cable, and a 5-V supply is used to power VA.

See Section 6 on page 20 regarding VA supply selection.

3 MASTER CLOCK CONFIGURATION

The CDB4244 offers many options for generating a system master clock. The master clock can be recovered from the incoming S/PDIF stream by the S/PDIF receiver or sourced from the socketed onboard oscillator in the event that the S/PDIF receiver's internal PLL becomes unlocked. This clock can be passed directly to the CS4244 and CS8406, or it can be passed through the CS2000 first to reduce jitter. Alternatively, the CS2000 can be used to generate a system master clock based on the onboard 16-MHz crystal. This option can be used to exercise 18 common master clock and sampling frequency combinations supported by the CS4244. Each of these options can be quickly realized using the FlexGUI software, with no change in hardware required. Figure 5 highlights how these components work together.
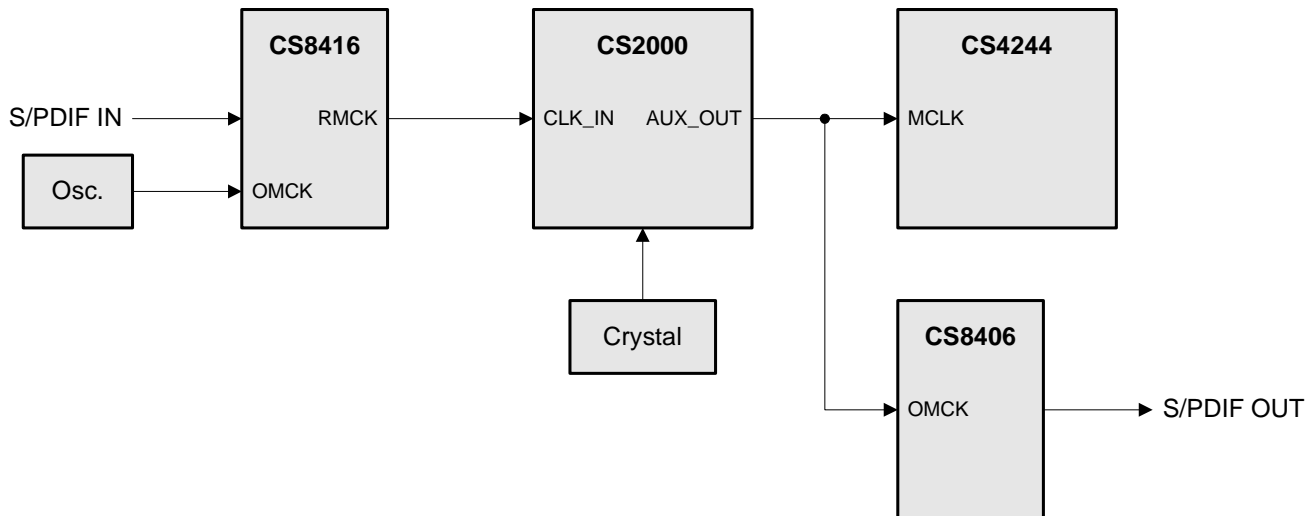
Figure 5. Master Clock Path

Note that the CS8416 S/PDIF receiver and the CS2000 are the only devices on the CDB4244 that can provide a system master clock. However, the S/PDIF receiver, S/PDIF transmitter, and CODEC are all capable of mastering system timing under the I²S and Left-Justified serial interface formats. Each device can be configured as master or slave using the FlexGUI software. It is the user's responsibility to ensure that only one device serves as master, with the remaining devices configured as slaves.

3.1 CS8416 Recovered Master Clock

By default, the master clock presented to the CS4244 and CS8406 is generated by the delta-sigma fractional-N frequency synthesizer of the CS2000. This low-jitter clock source is matched in frequency to the master clock recovered by the CS8416. The FlexGUI software enables this option at startup. This configuration can be restored by selecting the "CS8416 Recovered MCLK (Clean)" option under the "CS4244 and CS8406 MCLK Source" menu in the "Board Control" tab (see Section 2.1 on page 8 for more information).

In the event that the CS8416's internal PLL becomes unlocked, the CS8416 automatically sources the master clock from the socketed oscillator. This assumes the "Auto Clock Switching" box in the "CS8416 S/PDIF Receiver" group is checked. In this case, different master clock frequencies (and hence different sample rates) can be realized by replacing the socketed oscillator with oscillators of different frequencies.

Alternatively, the master clock recovered by the CS8416 can be passed directly to the CS4244 and CS8406 by choosing the "CS8416 Recovered MCLK (Raw)" option under the "CS4244 and CS8406 MCLK Source" menu. In this configuration, no jitter reduction is performed on the master clock presented to the CS4244 and CS8406. The CS2000 can be physically eliminated from the clocking path by removing all components pertaining to the CS2000 (U3, R25, C32, C33, C34, C35, Y1), and then populating R20 with a 0-Ω 0603 SMT resistor. Note that under this configuration, the "CS4244 and CS8406 MCLK Source" menu in the FlexGUI software has no effect.

3.2 CS2000-Generated Master Clock

For greater flexibility, the CS2000 can be configured to provide a master clock at several different frequencies. This eliminates the need to replace the socketed oscillator to achieve different sample rates in the event that the incoming S/PDIF stream is unavailable. Note that either the CS4244 or CS8406 must be configured as master in order to achieve different sample rates using the master clock generated by the CS2000. The CS8416 must be configured as slave or disabled to prevent contention on the LRCK and SCLK signals (refer to the CS8416 data sheet for more information). It is not recommended to exercise the digital-input-to-analog-output path (through the CS8416 and the CS4244 DACs) while the CS8416 is configured as slave, because the sample rate delivered to the CS8416 OLRCK input and the sample rate from the incoming S/PDIF stream are generated in two different clock domains. This may result in repeated or dropped samples, distorting the analog output signal produced by the CS4244.

Different master clock frequencies are realized by choosing one of the "CS2000 Generated..." options within the "CS4244 and CS8406 MCLK Source" menu in the "Board Control" tab of the FlexGUI software. Each option shows the master clock frequency, anticipated master-clock-to-sample-rate ratio, and the resulting sample rate. For example, "12.2880 MHz (256x48.0 kHz)" means that a sample rate of 48.0 kHz with an MCLK / F_S ratio equal to 256 results in a 12.2880-MHz master clock.

A total of 18 common master clock frequencies that are supported by the CS4244 are provided. It is the user's responsibility to ensure that the CS4244 is configured to accept the incoming master clock by making the appropriate changes in the "CODEC Control" tab of the FlexGUI software. See Section 2.2 on page 9 and the CS4244 data sheet for more information. Furthermore, the user must also ensure that the CS8406 is properly configured to match the relevant serial port settings of the CS4244 by making the appropriate changes in the "Board Control" tab (refer to the CS8406 data sheet for more information). Note that not all of the master-clock-to-sample-rate ratios that are supported by the CS4244 are supported by the CS8406. The remaining CS4244 combinations may only be exercised through external control (refer to Section 1.8 on page 5).

3.3 CS2000 Timing Reference

By default, the CS2000 uses a 16-MHz crystal to serve as the device's timing reference. Alternatively, this crystal can be removed so that the socketed 12.2880-MHz oscillator serves as the device's timing reference. This is accomplished by first removing the crystal (Y1) and capacitors C34 and C35, and then populating R24 with a 0-Ω 0603 SMT resistor. This routes the oscillator to the CS2000 timing reference clock input pin.

Note: The FlexGUI software and associated scripts assume the use of a 16-MHz timing reference. Changes to this frequency will alter the frequencies generated by the "CS2000 Generated..." options within the "CS4244 and CS8406 MCLK Source" menu. Furthermore, using a timing reference frequency other than that of the default 16-MHz crystal may require changes to the Reference Clock Input Divider register setting of the CS2000. Therefore, it is highly recommended that the crystal timing reference is not altered from its factory preset configuration. Refer to the CS2000 data sheet for more information.

3.4 Miscellaneous Options

The clock present on the timing reference pin of the CS2000 can act as the system master clock by selecting "External Timing Reference" under the "CS4244 and CS8406 MCLK Source" menu. Alternatively, the master clock can be disabled by selecting "OFF" from the same menu. This configures the auxiliary output of the CS2000 as high impedance.

4 ANALOG INPUT FILTERS

The CDB4244 makes it possible to realize two different analog input filter options for interfacing with the CS4244: a convenient active single-ended-to-differential filter to showcase maximum analog input performance, and an optional passive differential filter to minimize component count. Refer to *AN340: CS4234/4244 Filter Considerations* for a detailed discussion of the theory and design decisions behind each filter. The following sections highlight the use cases of each filter.

4.1 Active Single-Ended-to-Differential Input Filter

By default, the CDB4244 is configured with an active single-ended-to-differential input filter network on each input channel to allow a simple single-ended signal to be connected to each of the board's analog inputs. The filter network converts the single-ended signal into a differential signal to interface with the differential analog inputs of the CS4244, while minimizing source impedance in order to achieve maximum analog input performance. Figure 6 highlights the signal flow of this filter.
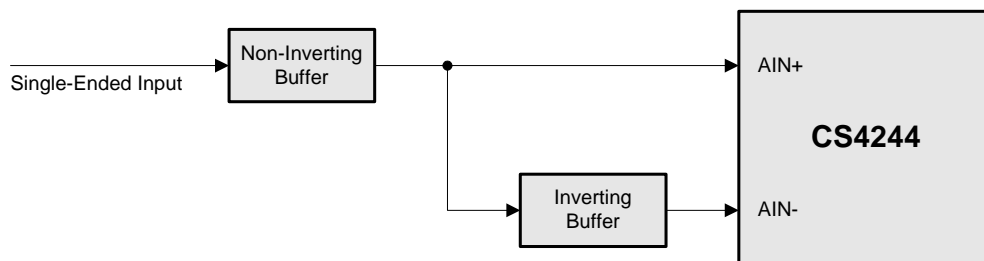
Figure 6. Active Single-Ended-to-Differential Input Filter Block Diagram

Use of this filter network requires a dual-rail ±12-V power supply to power the operational amplifiers employed in the design. Note that the amplitude of the single-ended input signal is doubled by the differential conversion. As such, the full-scale input voltage that can actually be applied at the input of the filter is 6 dB below the full-scale input voltage specified in the CS4244 data sheet.

4.2 Passive Differential Input Filter

Alternatively, each input channel of the CDB4244 can be configured with a passive differential input filter network to reduce component count at the cost of performance. In this configuration, a differential input signal is connected to each analog input of the CDB4244, filtered through a passive network, and presented directly to the CS4244 analog inputs. Figure 7 highlights the signal flow of this filter.
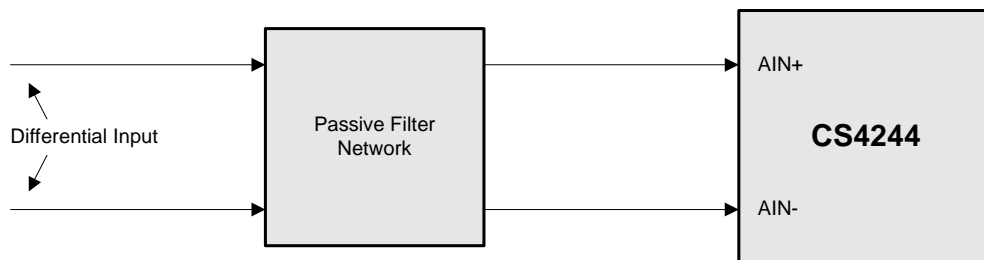
Figure 7. Passive Differential Input Filter Block Diagram

Because no active circuit elements are used in this design, the dual-rail ±12-V power supply can be removed completely if no active output filters are in use (refer to Section 5.1 on page 17). If only the +5-V power supply remains in use, the CDB4244 can be powered solely from the PC USB port when the board power is configured as specified in Table 4 on page 21.

Either filter option is realized by populating certain components and removing others. Section 4.3 contains a comprehensive list of components, and Figure 18 on page 31 contains a silk-screen diagram to aid in locating each component. Note that because of the grouping of the ADC common-mode voltages of the CS4244, the filter option used for AIN1 must also be used for AIN2. Likewise, the filter option used for AIN3 must also be used for AIN4. Refer to the CS4244 data sheet for more information.

4.3   Analog Input Filter Configuration

The following table lists the components that must be present or absent in order to realize either filter design for each of the four input channels. "POPULATE" or a component value specifies that the component should be populated, while "NO POP" specifies that the component should not be populated.

Reference Designator (AIN1, AIN2, AIN3, AIN4)	Description	Active S/E→Differential*	Passive Differential
C78, C43, C86, C139	Electrolytic, SMT Case B, 20% 16 V	4.7 µF	10 µF
C17, C69, C135, C155		NO POP	10 µF
C84, C47, C124, C152		22 µF	NO POP
C79, C44, C87, C140	C0G, SMT 0603, 5% 16 V	470 pF	NO POP
C80, C45, C88, C141		470 pF	NO POP
C41, C77, C137, C157		2700 pF	240 pF
C89, C48, C125, C153	X7R, SMT 0603, 5% 25 V	0.01 µF	NO POP
C122, C68, C134, C154		0.01 µF	NO POP
C82, C46, C123, C151		0.01 µF	NO POP
R29, R78, R207, R234	SMT 0603 (Note 1)	NO POP	100 kΩ
R26, R73, R203, R230		0 Ω	NO POP
R18, R72, R202, R229		0 Ω	NO POP
R12, R71, R201, R228		0 Ω	NO POP
R27, R74, R204, R231		NO POP	0 Ω
R30, R77, R206, R233		NO POP	0 Ω
R32, R88, R209, R236		0 Ω	2.0 kΩ
R33, R89, R210, R237		0 Ω	2.0 kΩ
R35, R91, R212, R239		NO POP	16.0 kΩ
R79, R36, R133, R213		634 Ω	NO POP
R81, R38, R135, R215		634 Ω	NO POP
R80, R37, R134, R214		634 Ω	NO POP
R83, R40, R137, R217		91 Ω	NO POP
R82, R39, R136, R216		91 Ω	NO POP
R84, R41, R138, R218		100 kΩ	NO POP
R86, R42, R139, R219		100 kΩ	NO POP
R87, R43, R140, R220		100 kΩ	NO POP
U5, U7, U10, U11	NE5532D, SOP-8	POPULATE	NO POP

*Default factory setting

Table 1. Analog Input Filter Components

Notes:

1.   Nonzero resistors are specified as 1/10 W with 1% tolerance.

5 ANALOG OUTPUT FILTERS

The CDB4244 allows the user to evaluate the CS4244 using five different output filter configurations: passive single ended, passive differential, active single ended, active differential, and active differential to single ended. Figure 8 demonstrates the available options on the board.
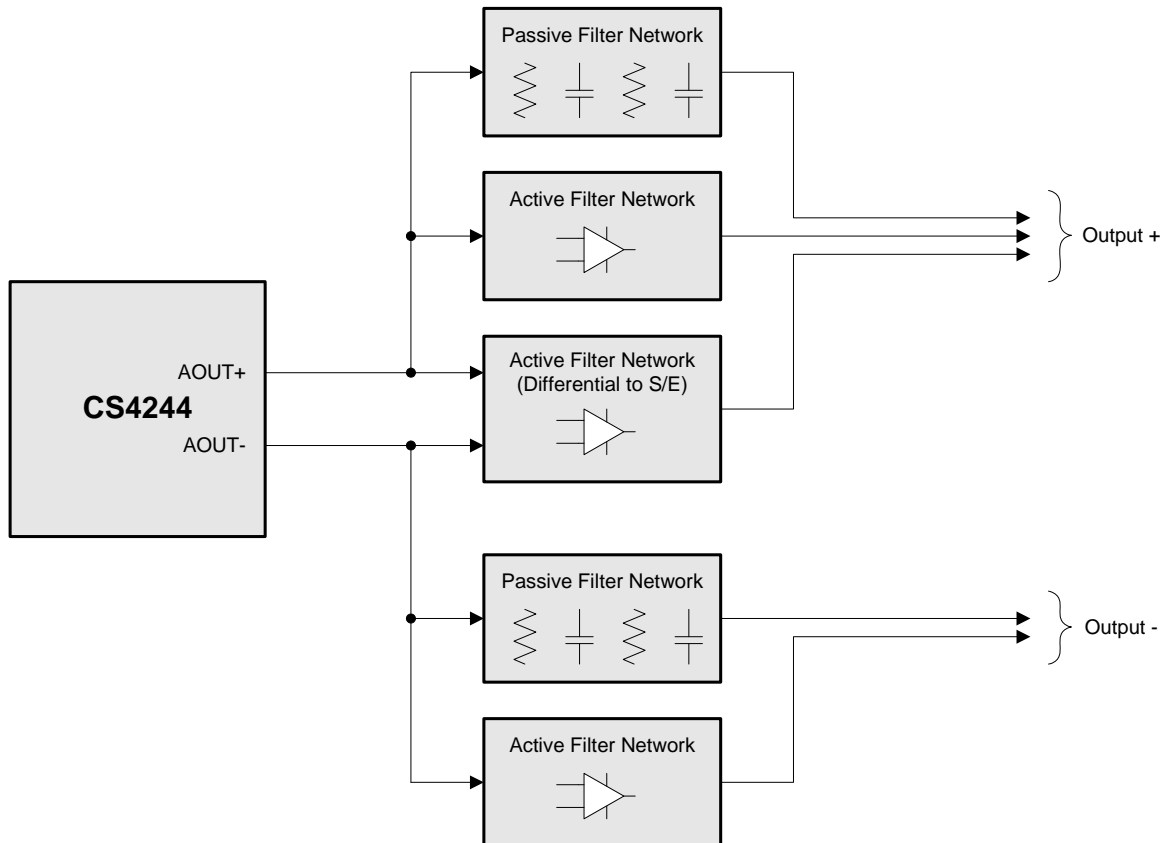
Figure 8. Analog Output Filter Block Diagram

Each output filter option is realized by populating certain components and removing others. Section 5.2 on page 19 contains a comprehensive list of components, and Figure 18 on page 31 contains a silk-screen diagram to aid in locating each component. By default, the CDB4244 is configured to use a passive differential filter on each output channel.

5.1 Analog Output Filter Considerations

If any of the three active output filter configurations are used, a dual-rail ±12-V supply must be connected to the CDB4244 to power the operational amplifiers used in these filter designs. The dual-rail supply is not required for the passive single-ended or differential output filter options, but is still required when using the default active single-ended-to-differential filter network on the input channels of the CDB4244. As mentioned in Section 4.2 on page 15, if every input and output channel is configured to use a passive filter network, the ±12-V supply may be removed.

The negative supply rail of the active output filter network can be tied to -12 V or ground to provide the option of a dual-rail or single-rail supply, respectively. The dual-rail supply is achieved by populating R141 with a 0-Ω 0603 SMT resistor and omitting R142. Omitting R141 and populating R142 allows for a single-rail supply. This is shown in Figure 17 on page 30. The CDB4244 is configured to use a dual-rail supply by default. Note, however, that exercising the single-rail supply option limits the voltage swing of the output signal. Driving a full-scale output signal with a single-rail supply severely clips the analog output signal.

Note that there is a phase reversal on the analog audio output connections of the CDB4244 when using an active output filter; this is due to the inverting amplifier configurations used in each design. This is noted along the three-pin differential output headers (see Section 6.1 on page 20) by the "+" and "-" labels next to the headers. There is no phase reversal for either passive filter configuration.

Loads connected to the analog outputs of the CS4244 must satisfy the device's minimum and maximum loading requirements. The active output filters that can be realized using the CDB4244 satisfy these requirements. However, the user must adhere to the minimum and maximum loading requirements of the CS4244 when connecting an external load to the CDB4244 while using a passive output filter. See Figure 15 on page 28 and Figure 16 on page 29 to observe the loads already present on the analog outputs of the CS4244 under the passive filter options, as these loads must be taken into account when connecting an external load to the CDB4244 using a passive output filter. See the CS4244 data sheet for the minimum and maximum loading specifications of the CS4244.

Refer to *AN340: CS4234/4244 Filter Considerations* for a detailed discussion of recommended output filters for the CS4244 as they pertain to the CDB4244. This document details the design decisions and trade-offs involved with the filters used here. Reference the CS4244 data sheet for the analog output characteristics of the device.

WARNING: The active differential-to-single-ended filter option places the full differential output voltage of the respective CS4244 analog output pair on a single RCA phono jack. Connect these outputs to external devices with caution, as this signal level may exceed the maximum allowable input amplitude for many consumer devices.

5.2 Analog Output Filter Configuration

The following table lists the components that must be present or absent in order to realize each filter design for each of the four output channels. "POPULATE" or a component value specifies that the component should be populated, while "NO POP" specifies that the component should not be populated.

Reference Designator (AOUT1, AOUT2, AOUT3, AOUT4)	Description	Passive Diff.*	Passive S/E	Active Diff.	Active S/E	Active D→S/E
C54, C95, C114, C162	Electrolytic, SMT Case B, 20% 16 V	22 µF	22 µF	NO POP	NO POP	NO POP
C60, C106, C129, C173		22 µF	NO POP	NO POP	NO POP	NO POP
C93, C110, C133, C177		NO POP	NO POP	22 µF	22 µF	NO POP
C56, C102, C121, C169		NO POP	NO POP	22 µF	NO POP	NO POP
C91, C108, C131, C175		NO POP	NO POP	22 µF	22 µF	22 µF
C92, C109, C132, C176		NO POP	NO POP	22 µF	NO POP	NO POP
C90, C101, C120, C168		NO POP	NO POP	NO POP	NO POP	22 µF
C55, C96, C115, C163	C0G, SMT 0603, 5% 16 V	1500 pF	1500 pF	NO POP	NO POP	NO POP
C61, C107, C130, C174		1500 pF	NO POP	NO POP	NO POP	NO POP
C51, C53, C113, C161		NO POP	NO POP	1000 pF	1000 pF	1000 pF
C59, C105, C128, C172		NO POP	NO POP	1000 pF	NO POP	NO POP
C49, C52, C112, C160		NO POP	NO POP	270 pF	270 pF	270 pF
C58, C104, C127, C171		NO POP	NO POP	270 pF	NO POP	NO POP
C66, C99, C118, C166		NO POP	NO POP	NO POP	NO POP	1000 pF
C67, C100, C119, C167		NO POP	NO POP	NO POP	NO POP	270 pF
C62, C97, C116, C164	X7R, SMT 0603, 5% 25 V	NO POP	NO POP	0.01 µF	0.01 µF	0.01 µF
C64, C98, C117, C165		NO POP	NO POP	0.01 µF	0.01 µF	0.01 µF
C94, C111, C159, C178		NO POP	NO POP	0.01 µF	0.01 µF	NO POP
C57, C103, C126, C170		NO POP	NO POP	0.01 µF	NO POP	NO POP
R53, R54, R130, R180	SMT 0603 (Note 2)	47 kΩ	47 kΩ	NO POP	NO POP	NO POP
R61, R112, R150, R243		47 kΩ	NO POP	NO POP	NO POP	NO POP
R52, R48, R129, R179		470 Ω	470 Ω	NO POP	NO POP	NO POP
R60, R111, R149, R242		470 Ω	NO POP	NO POP	NO POP	NO POP
R13, R46, R127, R177		NO POP	NO POP	5.76 kΩ	5.76 kΩ	5.76 kΩ
R44, R47, R128, R178		NO POP	NO POP	5.76 kΩ	5.76 kΩ	5.76 kΩ
R58, R109, R147, R240		NO POP	NO POP	5.76 kΩ	NO POP	NO POP
R59, R110, R148, R241		NO POP	NO POP	5.76 kΩ	0 Ω	0 Ω
R17, R45, R126, R176		NO POP	NO POP	2.8 kΩ	2.8 kΩ	2.8 kΩ
R57, R108, R146, R186		NO POP	NO POP	2.8 kΩ	0 Ω	0 Ω
R94, R115, R153, R246		NO POP	NO POP	100 kΩ	100 kΩ	NO POP
R95, R116, R154, R247		NO POP	NO POP	100 kΩ	100 kΩ	NO POP
R55, R96, R144, R184		NO POP	NO POP	100 kΩ	NO POP	NO POP
R56, R97, R145, R185		NO POP	NO POP	100 kΩ	0 Ω	0 Ω
R98, R113, R151, R244		NO POP	NO POP	47 kΩ	47 kΩ	47 kΩ
R100, R114, R152, R245		NO POP	NO POP	47 kΩ	NO POP	NO POP
R51, R93, R143, R183		NO POP	NO POP	NO POP	NO POP	5.76 kΩ
R49, R62, R131, R181		NO POP	NO POP	NO POP	NO POP	2.8 kΩ
R50, R92, R132, R182		NO POP	NO POP	NO POP	NO POP	5.76 kΩ
U9, U12, U13, U14	NE5532D, SOP-8	NO POP	NO POP	POPULATE	POPULATE	POPULATE

*Default factory setting

Table 2. Analog Output Filter Components

Notes:

2. Nonzero resistors are specified as 1/10 W with 1% tolerance.

6 SYSTEM CONNECTIONS AND JUMPER PIN BLOCKS

6.1   System Connections

Connector	Ref. Designator	Direction	Description
+5 V EXT	J15	Input	+5.0-V regulated power supply.
GND	J16	Input	System ground.
-12 V	J18	Input	-12.0-V regulated power supply.
+12 V	J17	Input	+12.0-V regulated power supply.
USB	J7	Input/Output	USB connection to PC for I²C control. See Note 3.
S/PDIF IN (Optical) S/PDIF IN (Coaxial)	J3 J4	Input	Digital audio input to CS8416.
S/PDIF OUT (Optical) S/PDIF OUT (Coaxial)	J6 J5	Output	Digital audio output from CS8406.
C2	J8	Input/Output	I/O for programming the microcontroller (U16).
Ext Control Connection	J1	Input/Output	Header for external access to CS4244 control port. See Note 4.
Ext Control Connection	J2	Input/Output	Header for external access to CS4244 serial audio signals. See Note 4.
AIN1 DIFF (Jack) AIN2 DIFF (Jack) AIN3 DIFF (Jack) AIN4 DIFF (Jack)	J25 J9 J12 J28	Input	1/8" stereo audio jacks for differential analog audio inputs. See Note 5.
AIN1 DIFF (Header) AIN2 DIFF (Header) AIN3 DIFF (Header) AIN4 DIFF (Header)	J27 J11 J14 J30	Input	Three-pin headers for differential analog audio inputs. See Note 6.
AIN1 AIN2 AIN3 AIN4	J26 J10 J13 J29	Input	RCA phono jacks for single-ended analog audio inputs.
AOUT1 DIFF (Jack) AOUT2 DIFF (Jack) AOUT3 DIFF (Jack) AOUT4 DIFF (Jack)	J19 J22 J31 J34	Output	1/8" stereo audio jacks for differential analog audio outputs. See Note 7.
AOUT1 DIFF (Header) AOUT2 DIFF (Header) AOUT3 DIFF (Header) AOUT4 DIFF (Header)	J21 J24 J33 J36	Output	Three-pin headers for differential analog audio outputs. See Note 7 and Note 8.
AOUT1 AOUT2 AOUT3 AOUT4	J20 J23 J32 J35	Output	RCA phono jacks for single-ended analog audio outputs. See Note 7 and Note 9.

Table 3. System Connections

Notes:

3. Connecting to the PC through a USB hub is not recommended.

4. See Section 1.8 on page 5 for more information on configuring these headers.

5. These connectors are part of the optional passive differential input filter network and are not used by default. Refer to Section 4.2 on page 15 for more information.

6. When using the default active single-ended-to-differential analog input filter, only the pins labelled "+" (signal) and "G" (ground) are used. When using the optional passive differential filter, all three pins are used. This connectivity is shown in Figure 13 on page 26 and Figure 14 on page 27.

7. Silk-screen labels are placed near these connectors to indicate the phase reversal between the active ("A") and passive ("P") configurations. See Section 5.1 on page 17 for more information.

8. When using an optional single-ended output filter, the single pin labelled "+" and "-" under the "A" and "P" columns respectively is ignored. This connectivity is shown in Figure 15 on page 28 and Figure 16 on page 29.

9. These connectors are intended for use with one of the optional single-ended output filters and are not used by default. Refer to Section 5 on page 17 for more information.

6.2 Jumper Pin Blocks

Label	Ref. Designator	Purpose	Position	Function Selected
+5V Select	J62	Selects +5-V voltage source.	POST* USB	Voltage source is +5 V EXT binding post. Voltage source is USB.
VA Select	J61	Selects VA voltage source. See Note 10.	+5V +3.3V*	VA is +5 V. VA is +3.3 V.
VA Current	J63	VA supply current measurement.	Open Closed*	1-Ω resistor placed in series in supply path. 1-Ω resistor is shorted. See Note 11.
VL Current	J64	VL supply current measurement.	Open Closed*	1-Ω resistor placed in series in supply path. 1-Ω resistor is shorted. See Note 11.

*Default factory setting

Table 4. Jumper Pin Blocks

Notes:

10. See the CS4244 data sheet for performance differences between VA supply levels.

11. J63 and J64 must be closed during normal operation.

6.3 Test Points

The CDB4244 contains several convenient test points for analyzing signals to and from the CS4244. A looped test point is available for each digital signal of the device's control port and audio serial port, adjacent to the respective external connection headers (J1 and J2, described in Table 3 on page 20). These test points are connected directly to the appropriate CS4244 pins and can be used both with external control (through the use of J1 and J2), or normal operation (J1 and J2 configured as described in Section 1.8 on page 5).

Test points are available for analog signals as well. The three-pin headers described in Table 3 on page 20 serve as breakouts to allow access to the raw analog input signals, or filtered analog output signals. Furthermore, two-pin headers (J41–J48) are available to observe the analog input and output pins of the CS4244.

Note: Headers J41–J48 should not be shunted. They are test points that have been designed using headers to simplify layout.

7 CDB4244 BLOCK DIAGRAM

Figure 12 on page 25

Figure 10 on page 23

USB Control Port

Control Header

Figure 11 on page 24

Figure 11 on page 24

Osc.

Crystal

Figure 10 on page 23

Analog Inputs
- Active Single Ended to Differential
- Passive Differential

Clock Synthesis (CS2000)

S/PDIF Input (CS8416)

Figure 11 on page 24

Figure 13 on page 26

Figure 14 on page 27

Figure 11 on page 24

CS4244

Figure 11 on page 24

S/PDIF Output (CS8406)

Analog Outputs
- Passive Single Ended & Differential
- Active Single Ended & Differential
- Active Differential to Single Ended

Figure 11 on page 24

Figure 15 on page 28

DSP Header

Figure 16 on page 29

Figure 10 on page 23

Figure 9. CDB4244 Block Diagram
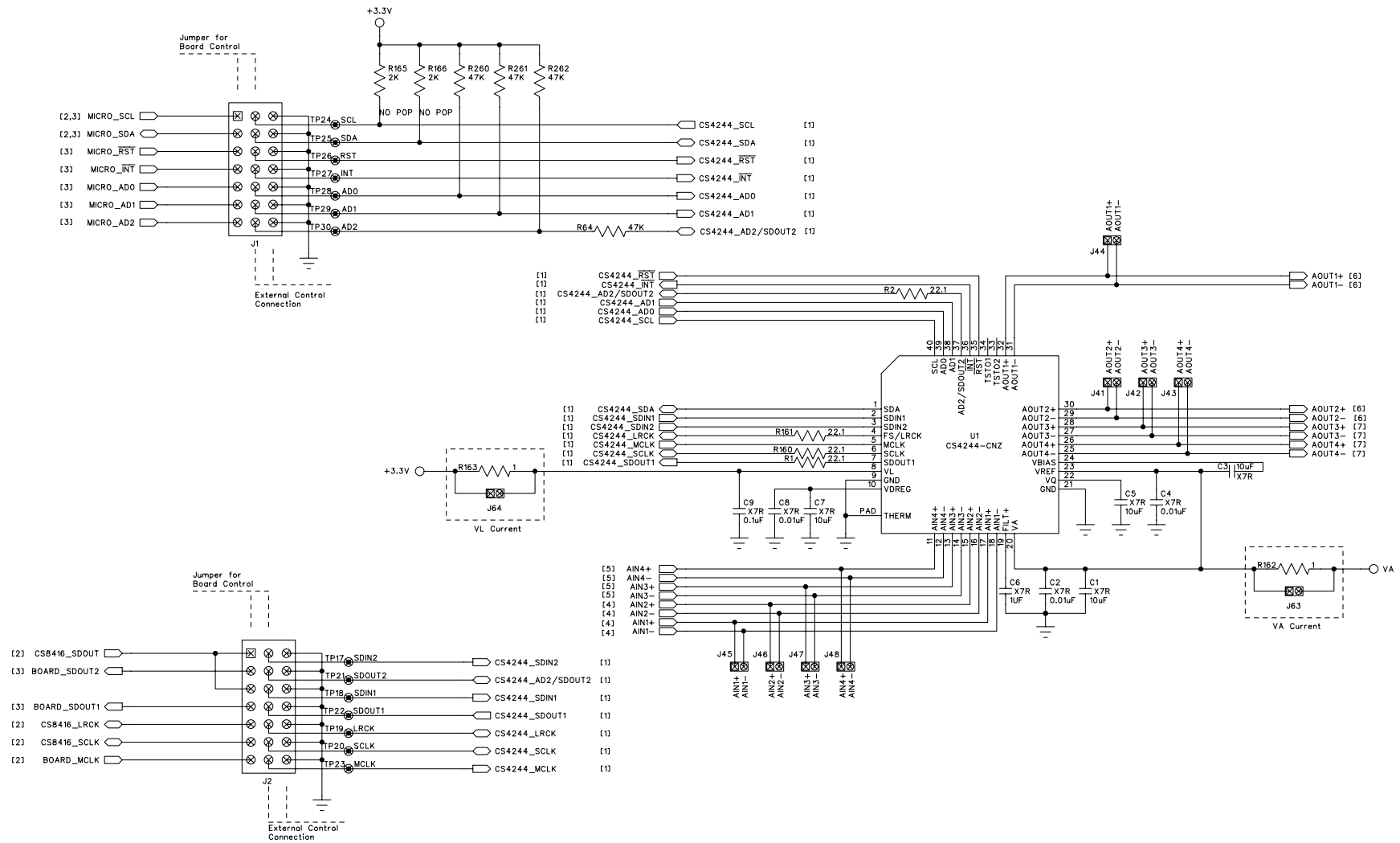
Figure 10. CS4244 (Schematic Sheet 1)

S/PDIF Receiver (I2C Address: 0x20)
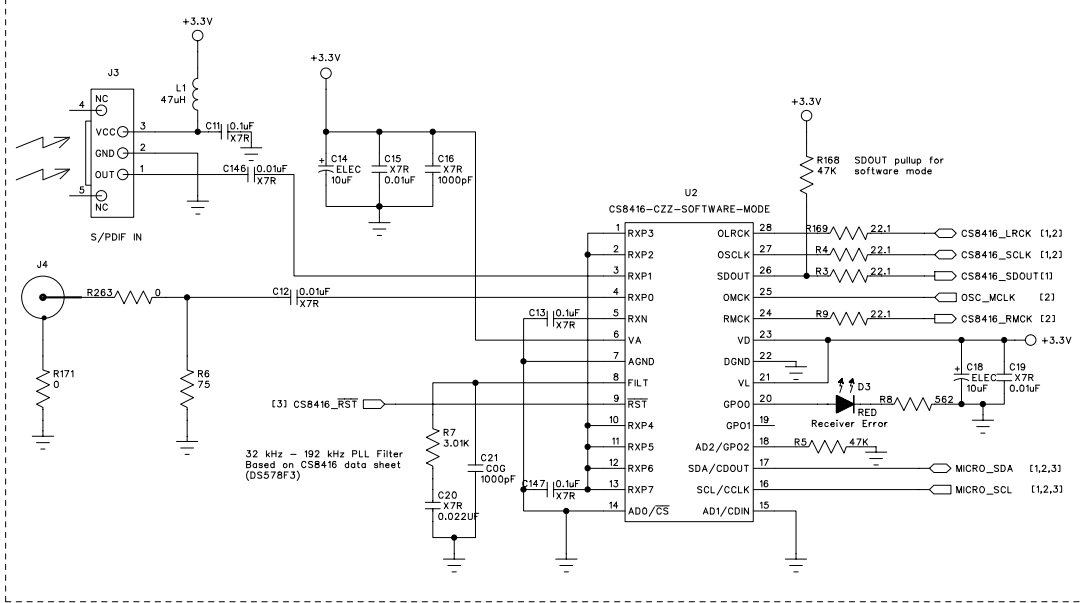
CS2000 (I2C Address: 0x9E)
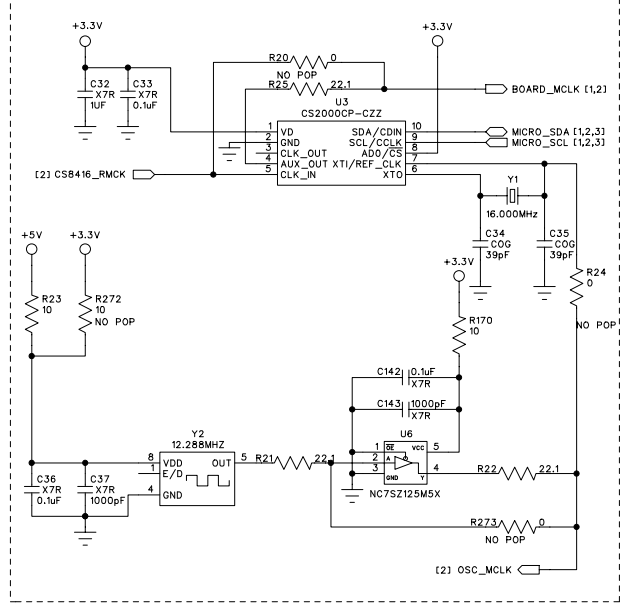
S/PDIF Transmitter (I2C Address: 0x28)
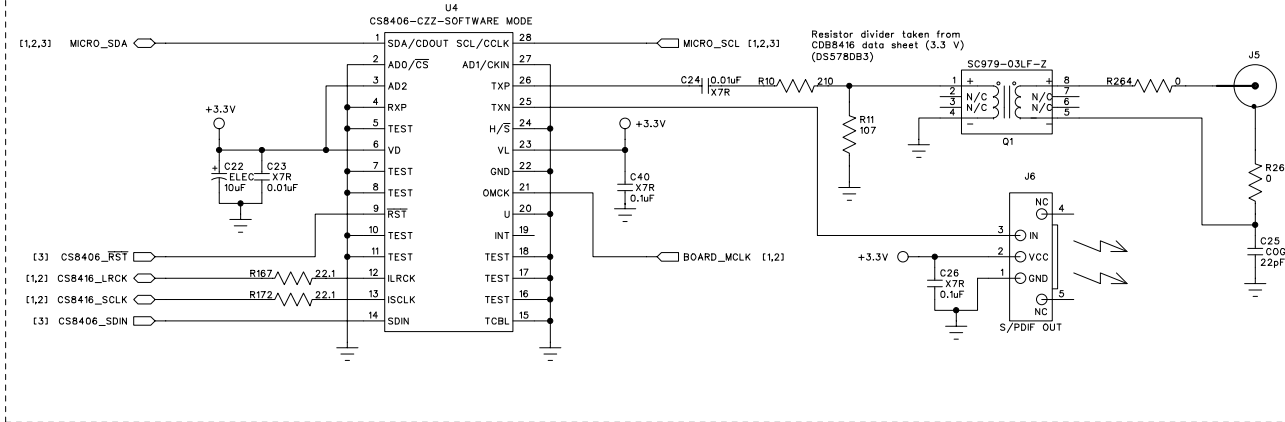
Figure 11. S/PDIF I/O (Schematic Sheet 2)

USB I/O
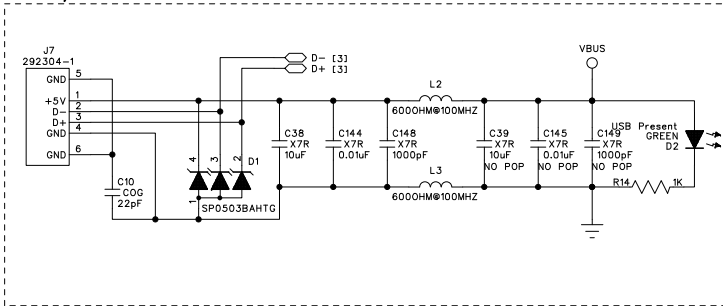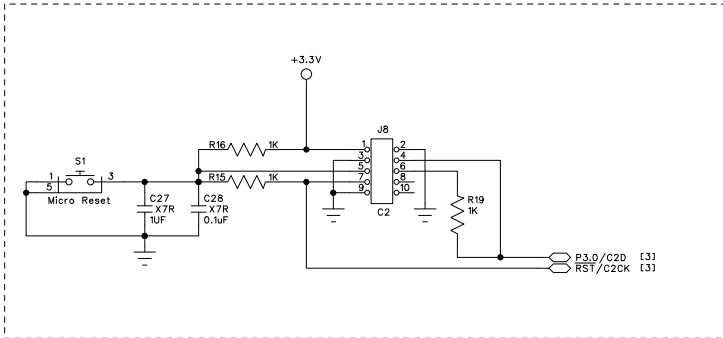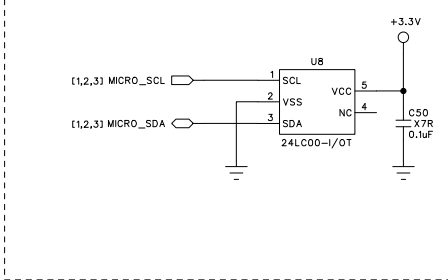
USB Microcontroller

Reset, C2

SDOUT Muxing

Board ID EEPROM
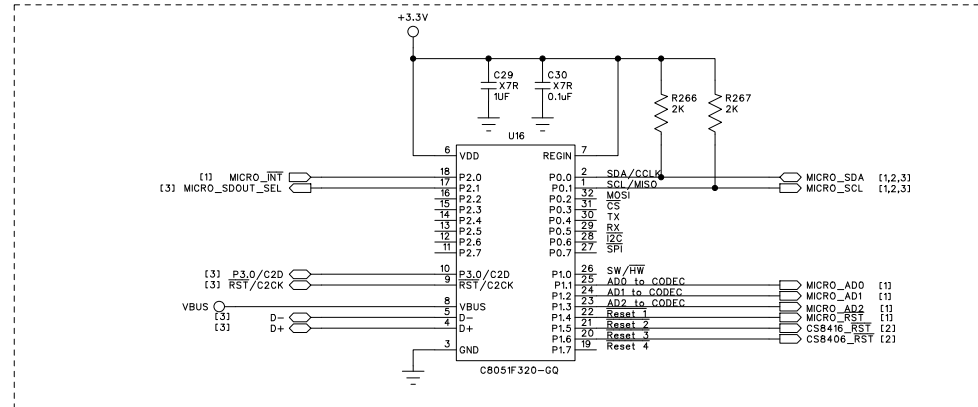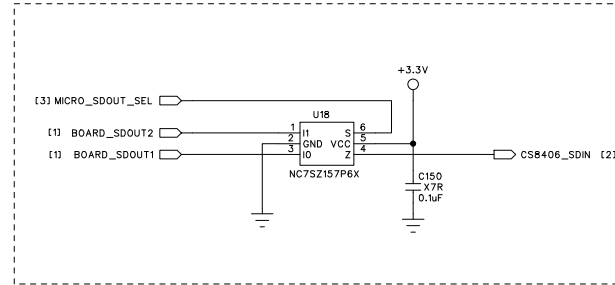
Figure 12. USB I/O (Schematic Sheet 3)

CDB4244
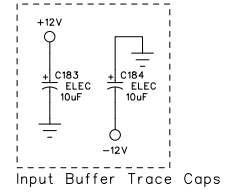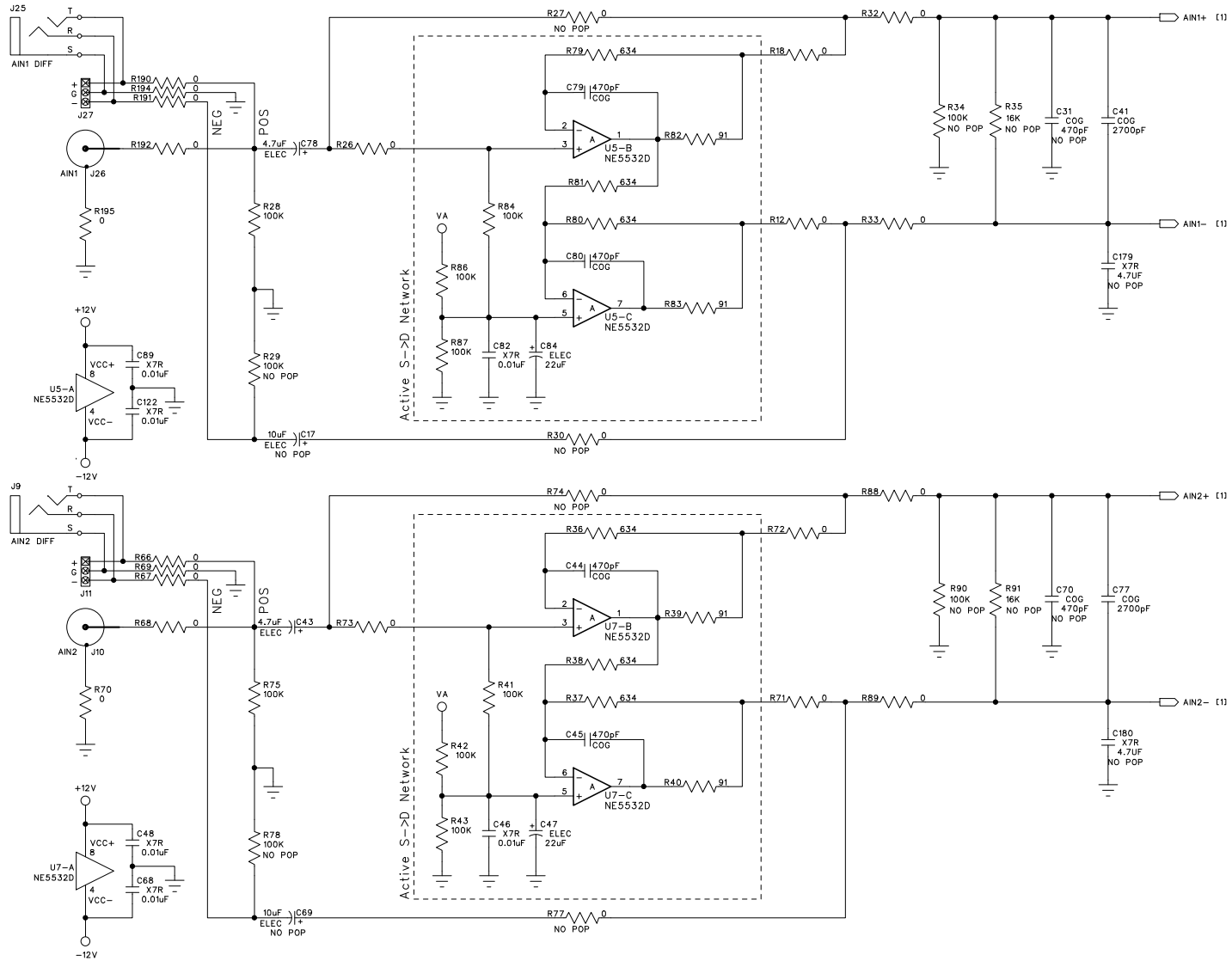
Figure 13. Analog Input Channels 1 & 2 (Schematic Sheet 4)
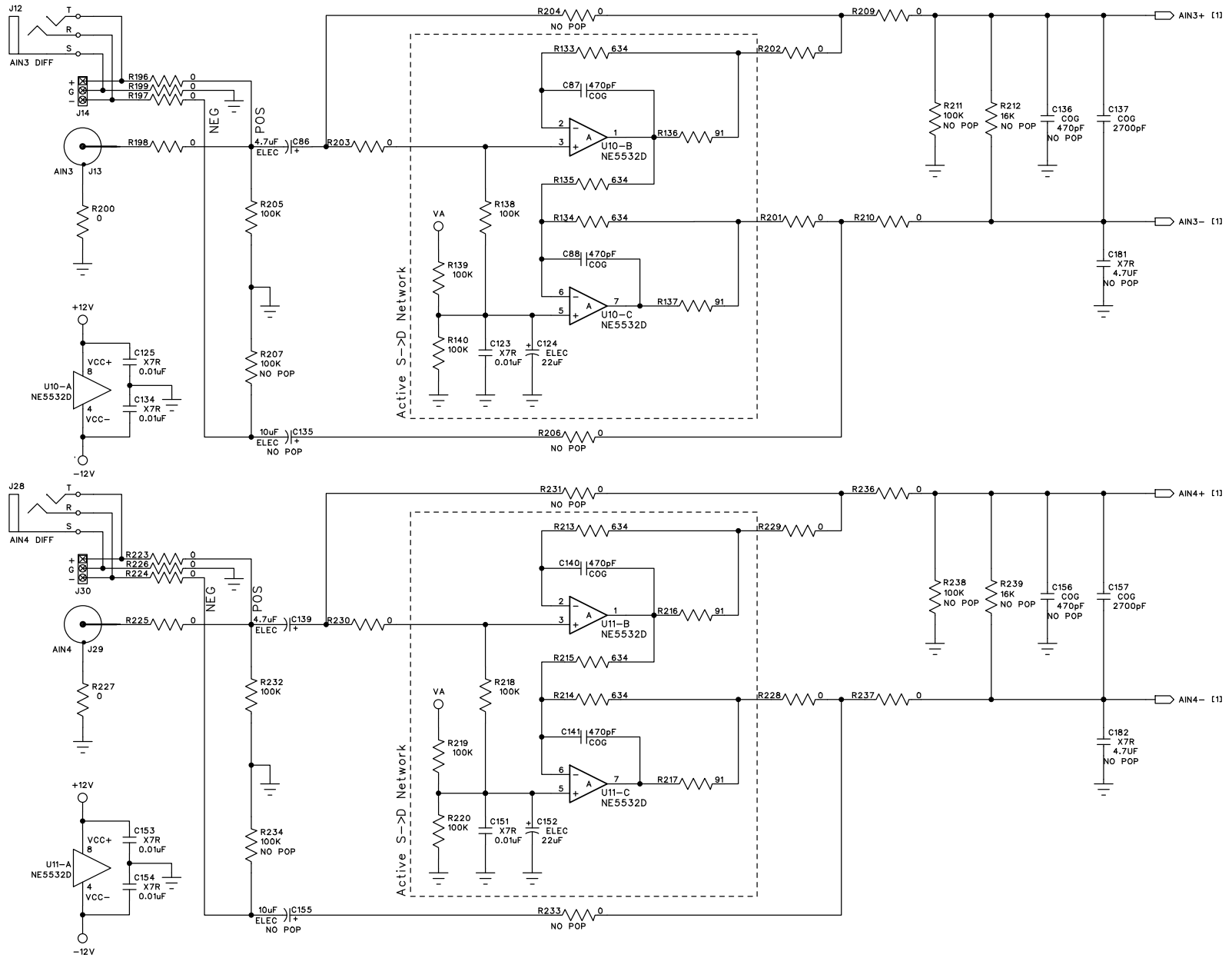
Figure 14. Analog Input Channels 3 & 4 (Schematic Sheet 5)
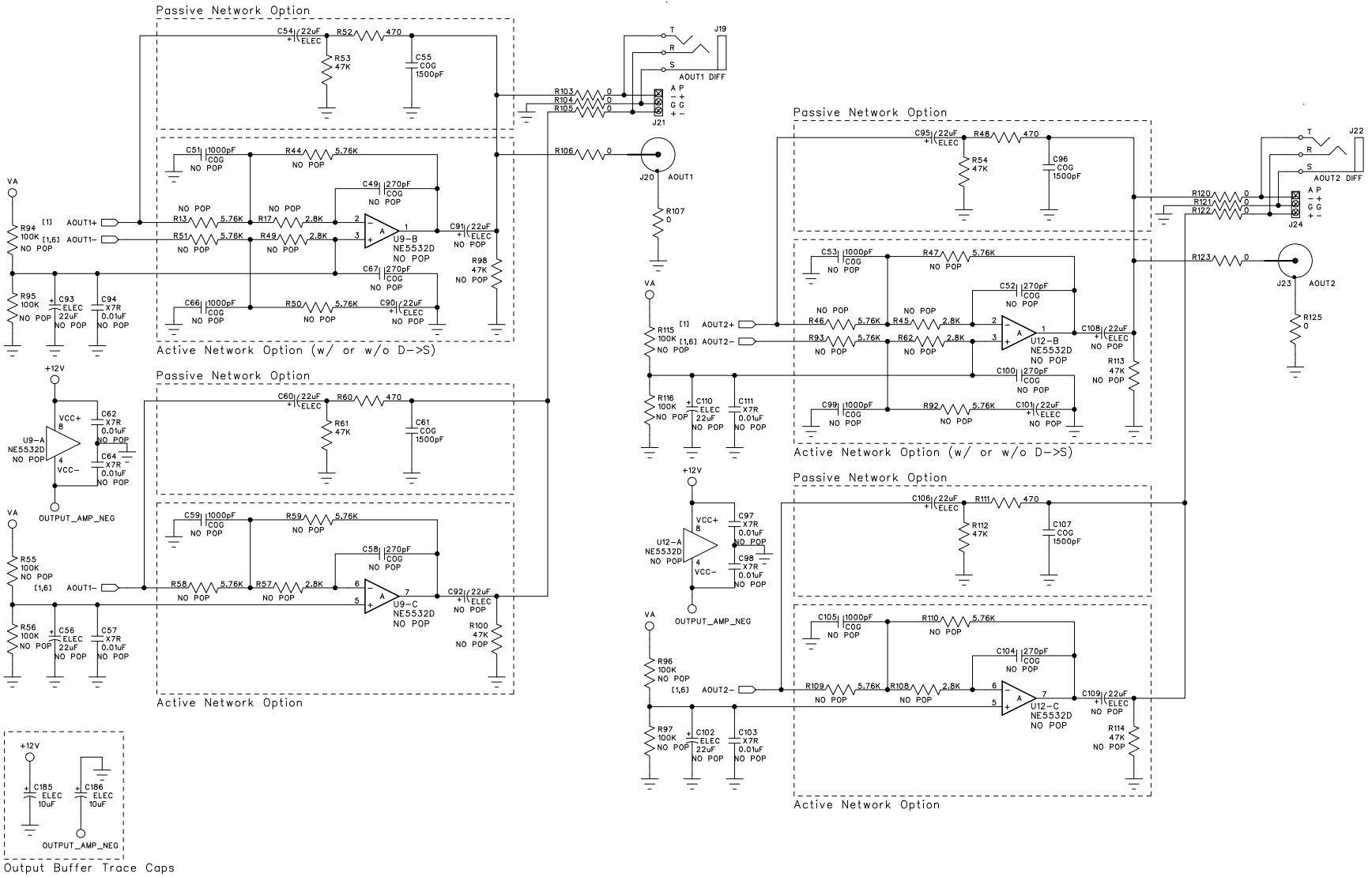
Figure 15. Analog Output Channels 1 & 2 (Schematic Sheet 6)
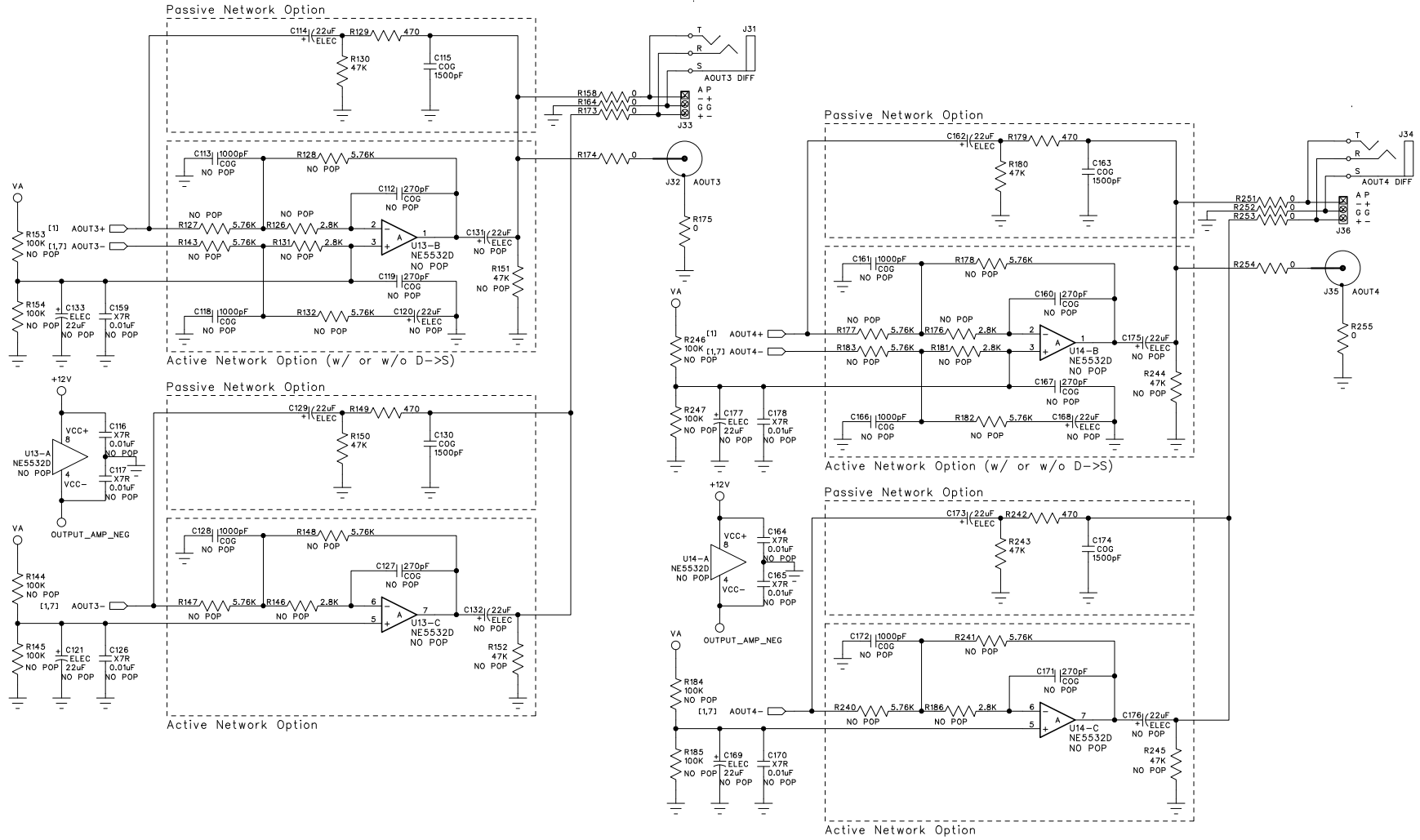
Figure 16. Analog Output Channels 3 & 4 (Schematic Sheet 7)

USB Power Option
(Passive Input/Output Only)

+5V_EXT   +5V   VBUS

1-2: EXT
2-3: USB

J62
+5V Select
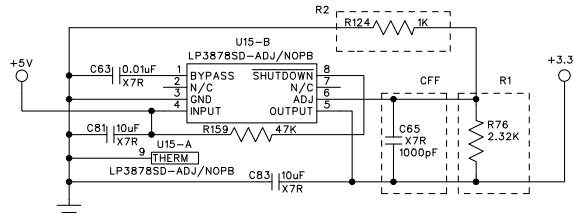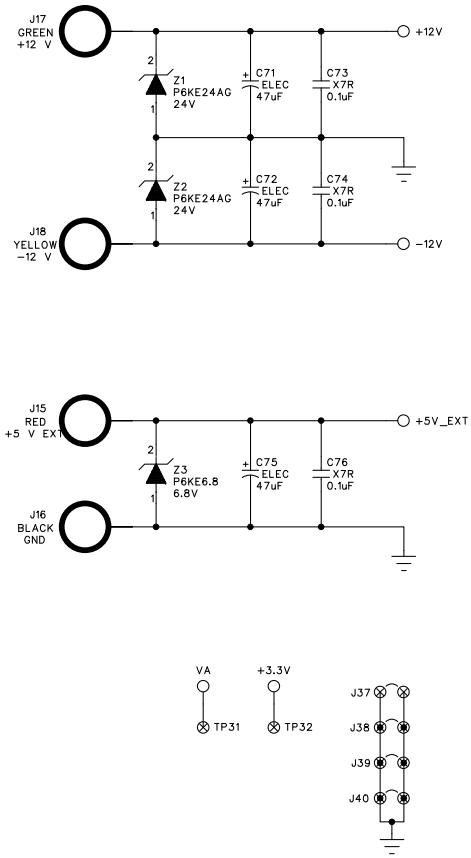
Regulator Design Notes

− Boxed R1, R2, CFF refer to LP3878−ADJ datasheet
− R1 & R2 selected for output = 3.32 V
− CFF & R1 selected for fz = 68.601 kHz

R2
R124 1K

U15−B
LP3878SD−ADJ/NOPB

C63 0.01uF
X7R

BYPASS   1   SHUTDOWN 8
N/C   2   N/C   7
GND   3   ADJ   6
INPUT   4   OUTPUT   5

CFF   R1

C81 10uF
X7R

R159 47K

U15−A
THERM
LP3878SD−ADJ/NOPB

C83 10uF
X7R

C65
X7R
1000pF

R76
2.32K

+3.3V
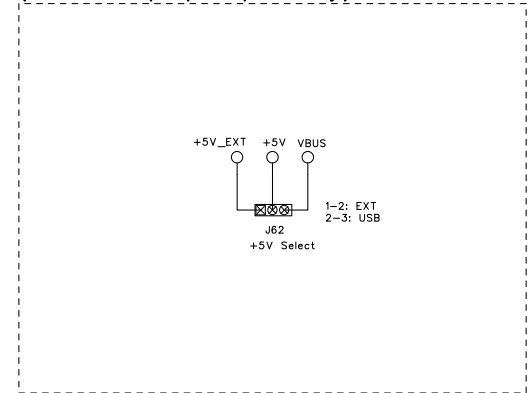
Single/Dual Rail Active Output Option

OUTPUT_AMP_NEG

Pop for Dual−Rail Active Output
R141 0

Pop for Single−Rail Active Output
R142 0

NO POP

−12V

VA Rail Selection

+3.3V VA +5V

1-2: +3.3 V
2-3: +5 V

J61
VA Select

J17
GREEN
+12 V

2
Z1
P6KE24AG
24V
1

C71
ELEC
47uF

C73
X7R
0.1uF

+12V

J18
YELLOW
−12 V

2
Z2
P6KE24AG
24V
1

C72
ELEC
47uF

C74
X7R
0.1uF

−12V

J15
RED
+5 V EXT

2
Z3
P6KE6.8
6.8V
1

C75
ELEC
47uF

C76
X7R
0.1uF

+5V_EXT

J16
BLACK
GND

VA   +3.3V
TP31   TP32

J37
J38
J39
J40
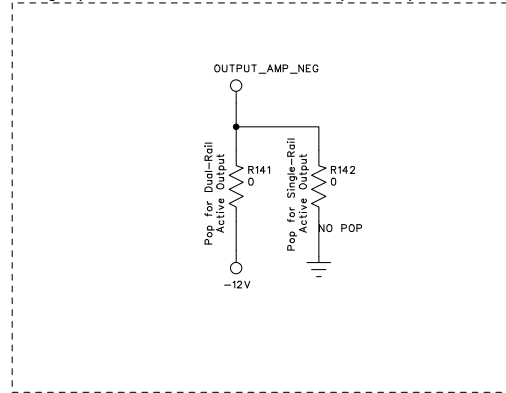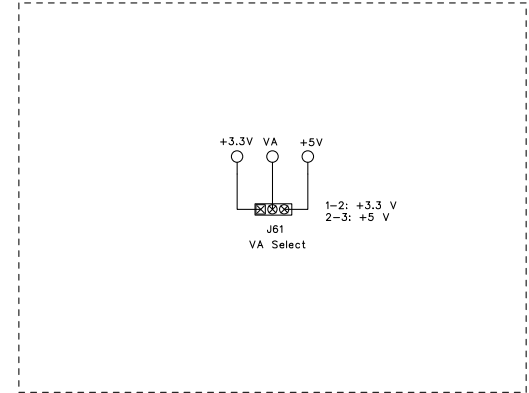
AUXILIARY HARDWARE AND RELATED DOCUMENTATION:

FD1   FD2   FD3

MH1   MH2   MH3   MH4

SCREW−PHILIPS−4−40THR−PH−5/16−L−Z
WIRE HOOK UP #6AWG STR BLU NPb
SOCKET 1P− 8134−HC−5P2
SHUNT_2P− 15−29−1025

PCB DWG− 240−00389−Z1
ASSY DWG− 603−00389−Z1
SCH DWG− 600−00389−Z1
LBL SUBASSY PROD ID AND REV

Figure 17. Power (Schematic Sheet 8)

PCB 240-00389-Z1 REV B
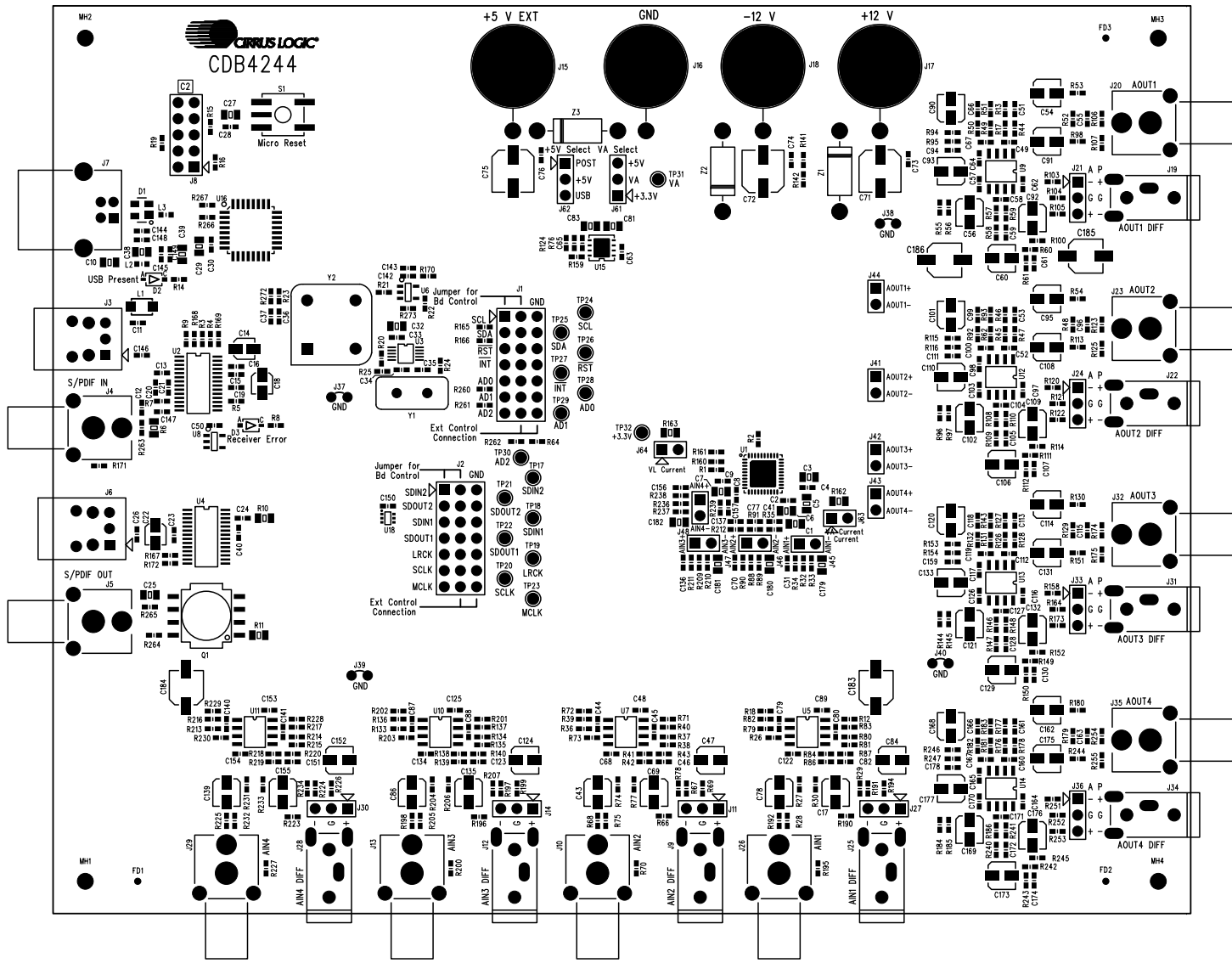
Figure 18. Silk Screen

CDB4244
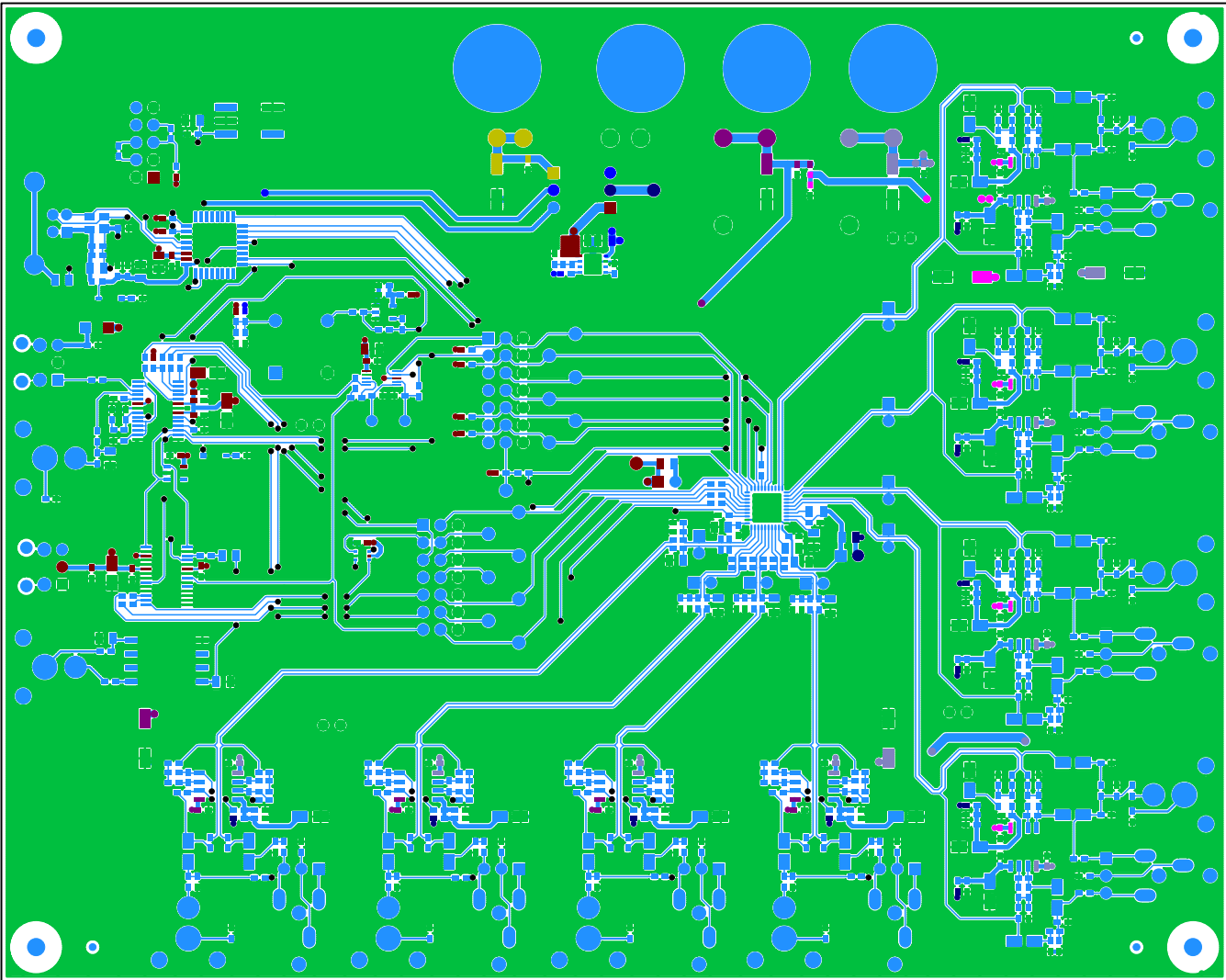
PCB 240-00389-Z1 REV B

Figure 19. Top Side (Layer 1)
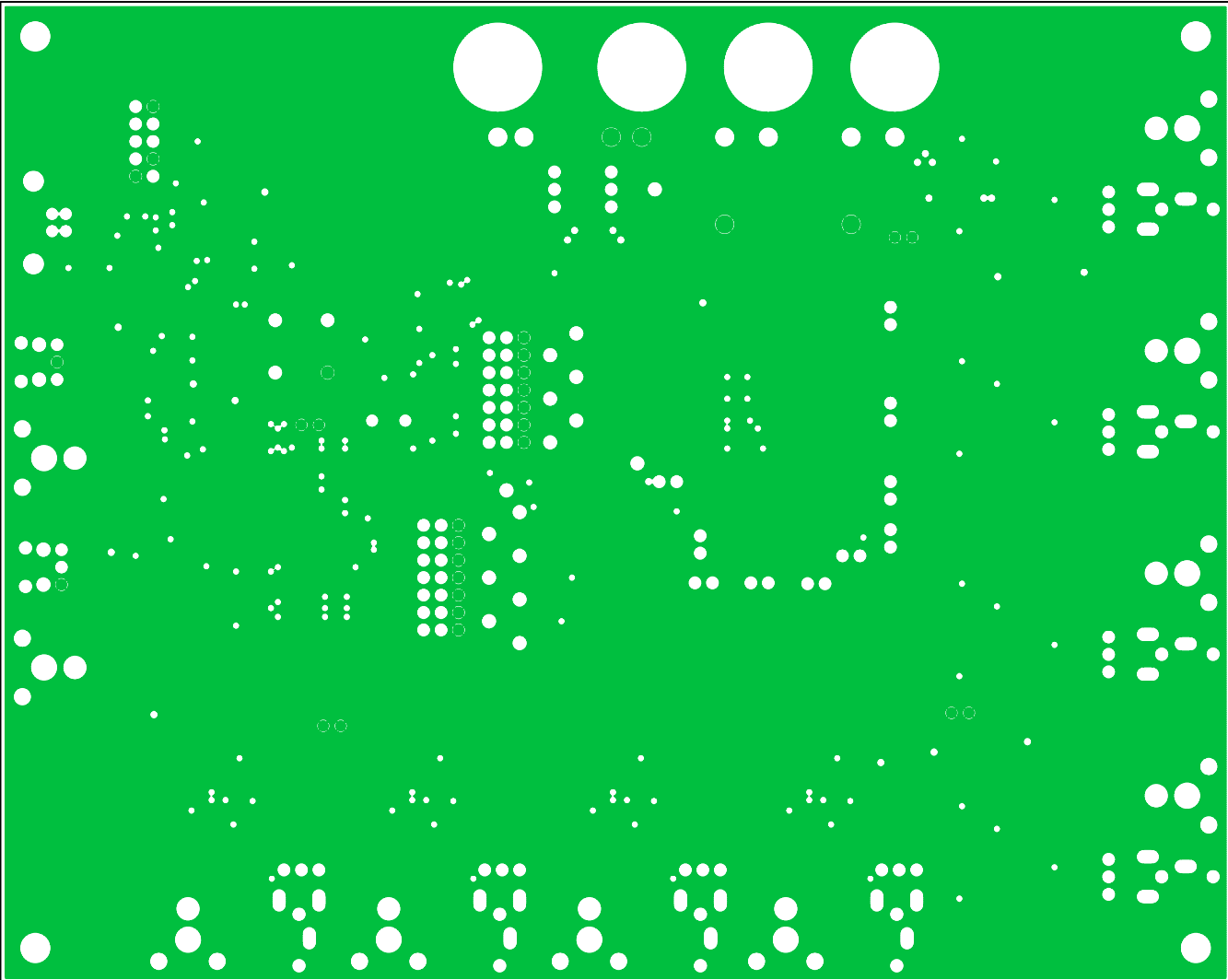
PCB 240-00389-Z1 REV B

Figure 20. Ground Plane (Layer 2)

CDB4244
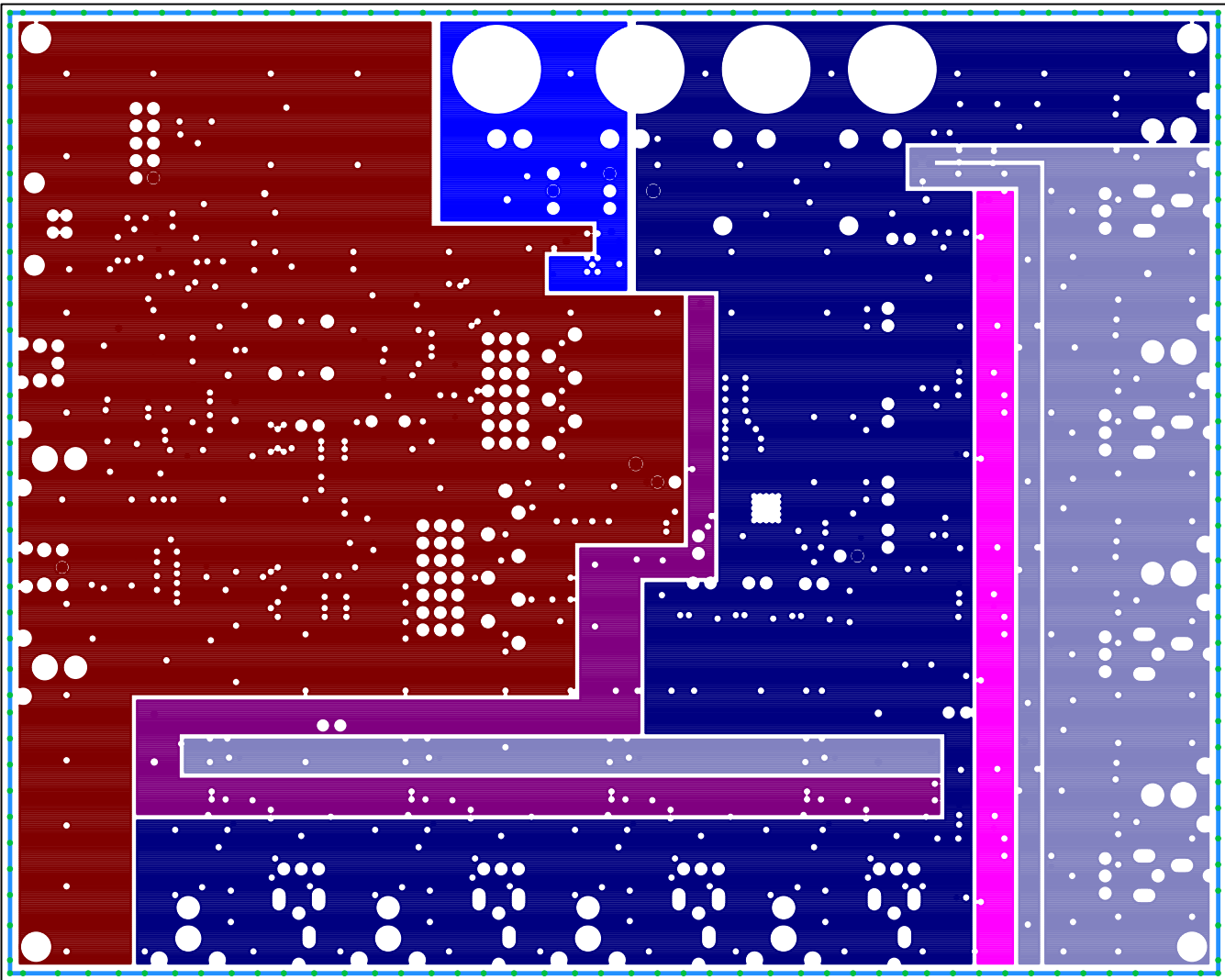
PCB 240-00389-Z1 REV B

Figure 21. Power Plane (Layer 3)
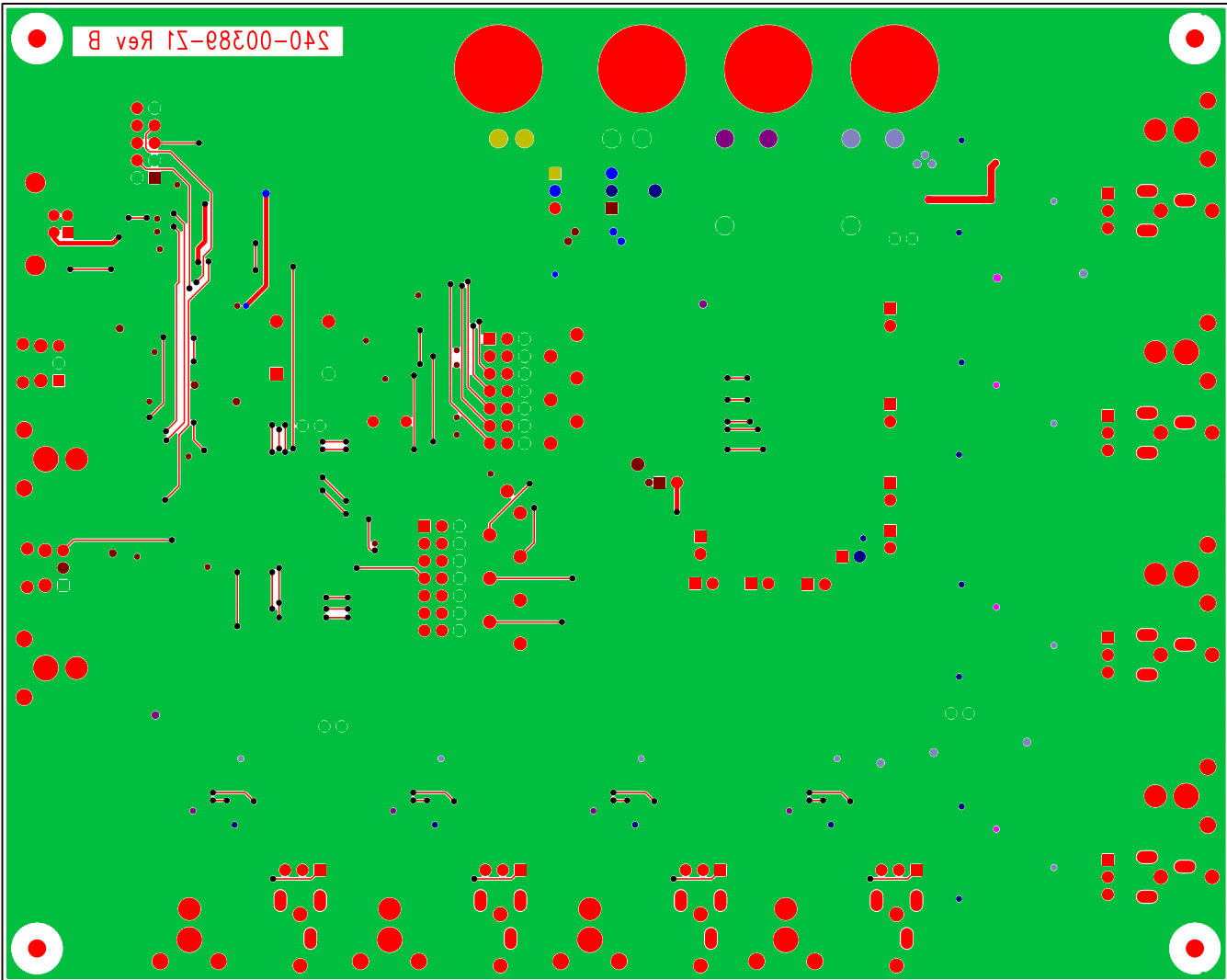
240-00389-Z1 Rev B

PCB 240-00389-Z1 REV B

Figure 22. Bottom Side (Layer 4)

10 REVISION HISTORY

Revision	Changes
DB1	– Initial Release
DB2	– Updated "Features" on page 1 to remove list of optional single-ended input filters. – Added description of interrupt pull-up behavior in Section 1.8 on page 5. – Removed single-ended input filter descriptions from Section 1.9 on page 6. – Updated Section 1.10 on page 6. – Updated Section 2 to reflect latest FlexGUI software version. – Updated Figure 5 on page 13. – Updated Section 3.1 on page 13. – Updated Section 3.2 on page 14. – Removed single-ended filter descriptions from Section 4. – Added Section 4.1 and Section 4.2 on page 15. – Removed single-ended input filter configurations from Table 1 on page 16. – Updated capacitor voltage ratings in Table 1 on page 16 and Table 2 on page 19. – Updated Figure 8 on page 17. – Updated Section 5.1 on page 17. – Changed label of connector J8 in Table 3 on page 20 and Figure 12 on page 25. – Added Note 5, Note 6, Note 8, and Note 9 under Table 3 on page 20. – Changed default position of jumper J61 in Table 4 on page 21. – Updated Figure 9 on page 22. – Added R25 to Figure 11 on page 24. – Updated Section 9 to reflect latest PCB layout.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest you, go to www.cirrus.com.