Continuous-Time Converter Architectures for Integrated Audio Processors:

By Brian Trotter, Cirrus Logic, Inc.

September 2008

As consumer electronics devices continue to both decrease in size and increase in complexity, there is a strong drive to integrate more and more functions onto a single chip. Reasons for this integration are numerous. Board design becomes simpler, with fewer devices to place and less interconnect to route. Power can be saved by driving small internal loads, rather than the larger loads seen driving out onto a board and to another device. Additionally, costs come down for both semiconductor suppliers and end customers.

In purely digital environments, integration has progressed at a furious pace. Over the last 10 years, digital integration has radically changed the system design of consumer electronics components such as DVD players, AVRs, and MP3 players. Consumers have reaped the benefits of faster, cheaper, and smaller consumer electronics devices. This integration path becomes much more difficult when one attempts to merge the analog and digital portions of the signal path. In many consumer electronics applications, large digital system-on-chip (SoC) ICs have begun to include this analog functionality. The challenge here is extreme. Despite many process enhancements such as deep n-well technology, which isolates the analog circuits from the digital core, a designer is ultimately trying to place a high performance analog converter on the same substrate as a fast and noisy digital signal processor (DSP). To date, few devices have made it to market with true high-performance converters and high-speed DSPs. In order to address this challenge, it is necessary to investigate new converter architectures which are less sensitive to interference from on-chip digital circuits.

CIRRUS LOGIC, INC.
2901 Via Fortuna
Austin, Texas 78746
United States
T +1-512-851-4000
F +1-512-851-4977
Toll-Free +1-800-888-5016

SALES SUPPORT
North America +1 800-625-4084
Asia Pacific +852 2376-0801
Japan +81 (3) 5226-7757
Europe/UK +44 (90) 1628-891-300

LEARN MORE AT
www.cirrus.com

TRADITIONAL SWITCHED-CAPACITOR ARCHITECTURE

The majority of modern audio converters utilize a switched capacitor architecture. Figure 1 shows a block diagram of a simplified switched-capacitor analog-to-digital converter (ADC).[1]

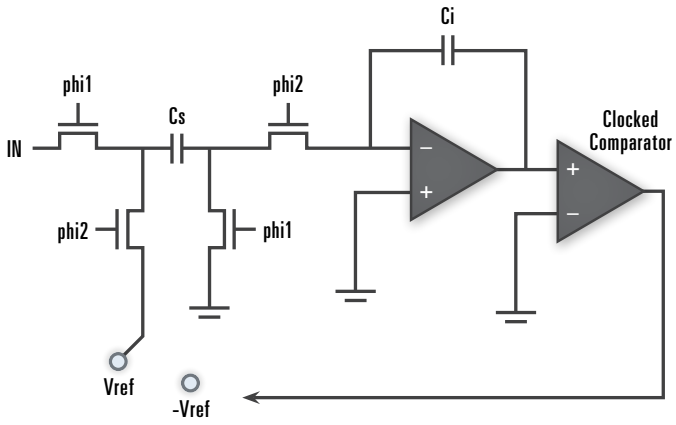

Figure 1. Standard Switched-Capacitor ADC

The architecture of a switched-capacitor digital-to-analog converter (DAC) is similar, and while the subsequent discussion will focus on the ADC, the analysis also applies to the DAC. In the ADC, the input audio signal is sampled onto a sampling capacitor (C_s), and then transferred to an integrating capacitor (C_i). A two-phase clock is used, where the input is sampled on phi1, and transferred to the integrating capacitor along with the feedback signal, ±Vref, on phi2. The critical time for this architecture is when the phi1 switches open, and the phi2 switches close. This is the point when the input signal is sampled and presented to the integrator. Any noise on the input or the ground will be sampled and appear at the ADC output. A common technique in converter design is to time the digital clock to occur after the sampling event.[2] Figure 2 shows an example of the timing of digital and analog clocks.

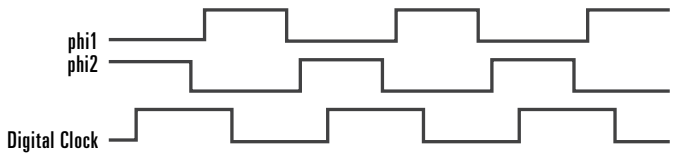

Figure 2. Switched-Capacitor Timing Diagram

The edges of the digital clock will invariably inject signal-dependent noise into the substrate, which will find its way to a reference node, or the ground node of the sampling capacitor. As long as the digital edge occurs after the sampling event, none of that noise will be sampled at the ADC input.

In a standalone converter, this noise management is easy to implement. All clocks are typically derived from a single source, so ensuring timing relationships between analog and digital clocks is straightforward. Even when the digital clock is faster than the analog clocks, it is not difficult to find safe areas to place those digital edges. On a complex DSP, where an asynchronous digital core may be running much faster than the converters, the problem is much harder. Figure 3 shows the nature of the problem.

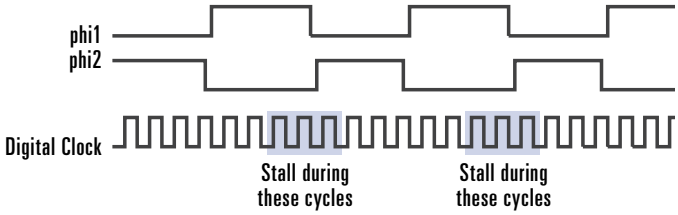

Figure 3. Switched-Capacitor Timing Diagram with Fast Digital Clock

There is no way to guarantee a safe time for the sampling event. In some solutions, the DSP is simply stalled for a number of cycles to create a safe sampling event,[3] as shown in the shaded boxes in Figure 3. This can effectively eliminate coupling between the DSP and the converters, but it comes at the cost of MIPS. Assume a typical 6.144 MHz converter clock, and a 98.3 MHz DSP clock (16x the converter clock). If one chooses to stall the processor for 3 clocks, to ensure some margin around the sampling event, this costs almost 20% of the chip's processing power.

A NEW CONTINUOUS-TIME ARCHITECTURE

A continuous-time architecture addresses many of these issues which limit the performance of integrated switched-capacitor converters. A block diagram of the new ADC architecture is shown in Figure 4.

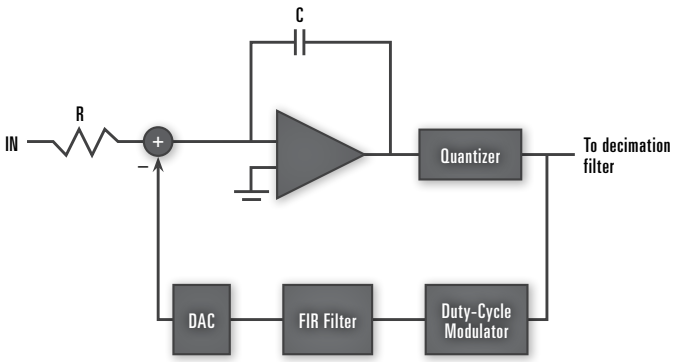

Figure 4. Continuous-Time ADC Architecture

As the integrators are all continuous-time, there is no critical sampling point on the input, and thus no need to stall the processor or find a safe edge for clocking the converter. The only sampling occurs at the quantizer output, which is another advantage since any coupled noise at this point has been filtered by the upstream integrator stages. This new architecture is not without its challenges. The traditional challenge with continuous-time architectures is that they are highly jitter sensitive. The FIR filter in the feedback path of the continuous-time ADC attenuates out-of-band noise significantly to reduce susceptibility to jitter. In the case of the DAC, there are additional advantages to the duty-cycle modulator and FIR filter in the path. Referring now to Figure 5, the continuous-time DAC architecture, using a duty-cycle modulator feeding an FIR filter adds filtering of out-of-band noise, and removes the need for dynamic element matching (DEM), since all elements are used during every conversion. Without the need for a DEM, the DAC can be built of hundreds of current elements, which attenuate noise and limit step size into the output amplifier, and scale with process much better than capacitor elements.

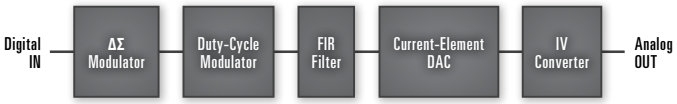

Figure 5. Continuous-Time DAC Architecture

This continuous-time architecture does depart from two of the hallmark advantages of the switched-capacitor converter: (1) reliance on capacitor ratios and (2) allowance for non-linear operation during settling. First, the parameters of a switched-capacitor design are set by a ratio of capacitors. While absolute capacitance values are not well controlled, capacitor ratios adhere to very tight tolerances in modern CMOS processes. In continuous-time designs, those same parameters are set by an RC product, which is not well controlled. A simple calibration is required to ensure the frequency response is unchanged across normal process variations. Secondly, switched-capacitor designs allow for simplified design of integrator amplifiers, as long as their outputs are sufficiently settled when switches are flipped. In the continuous-time architecture, care must be taken to ensure all amplifiers remain linear at all times.

EXPERIMENTAL RESULTS

Using a continuous-time architecture, it is now possible to integrate true high performance audio converters with a high speed DSP. In spite of all the challenges, experimental results confirm that this new converter architecture is indeed remarkably immune to noise generated by the DSP. This architecture was first implemented on the CS47048, a 150MHz audio DSP, with 4 integrated ADC channels, and 8 integrated DAC channels. The following plots demonstrate the performance of this device under various conditions. All performance plots were creating using a standard Audio Precision® system.

EXPERIMENTAL RESULTS (CONTINUED)

Figure 6 shows an FFT for a -60 dB input signal to the ADC. In this case, the DSP processor is largely off, only performing the operations necessary to move the data from the ADC output to an I²S output port.

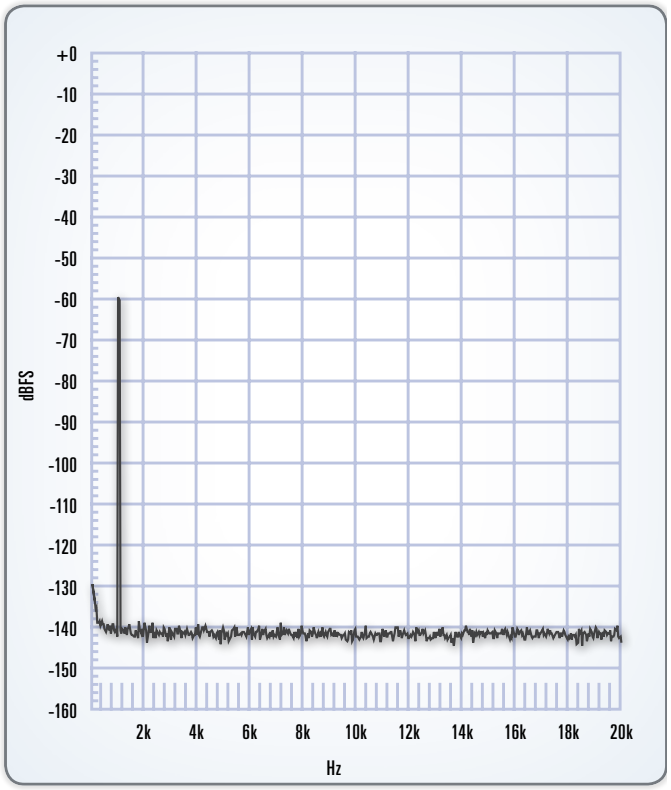

Figure 6. ADC Performance at -60dB Input Level with DSP Disabled

Similar analysis is shown for the DAC. Figure 7 shows an FFT for a -60 dB input signal to the DAC, with the DSP disabled.

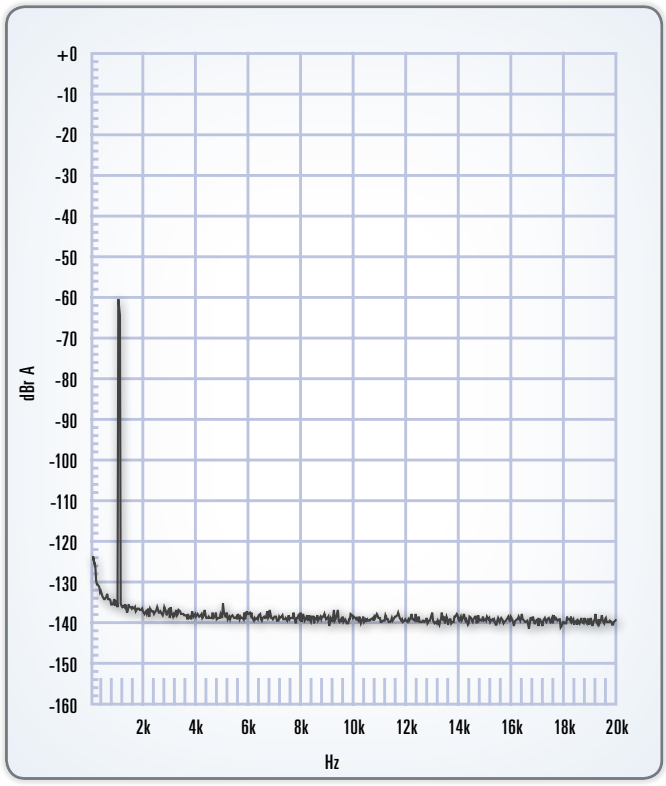

Figure 7. DAC Performance at -60dB Input Level with DSP Disabled

For both the ADC and the DAC, the noise floor is very clean, which is what we would expect with minimal interference from the on-chip DSP. The DAC Dynamic Range across the 20 Hz - 20 kHz band is 110 dB (A-weighted), and the ADC Dynamic Range across the same band is 111 dB (A-weighted).

The true benefits of the new continuous-time architecture are seen in the next plots, when the DSP core is enabled and running an intensive algorithm to inject large amounts of noise into the substrate.

EXPERIMENTAL RESULTS (CONTINUED)

Figure 8 shows the same -60 dB input signal to the DAC, but now with the DSP enabled, running the Dolby® Pro Logic® IIx + Dolby Headphone® 2 algorithm at a DSP clock rate of 150 MHz.

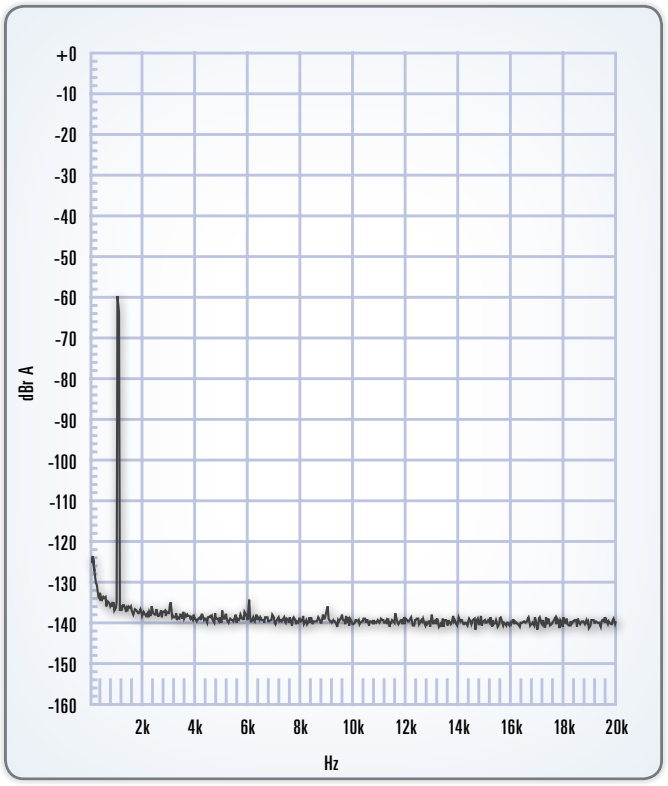

Figure 8. DAC Performance for -60dB Input Level with DSP Enabled

There is very little additional interference in the noise floor, and all tones and harmonics are well below the -130 dB level. Overall Dynamic Range Performance still 110 dB (A-weighted) across the 20 Hz - 20 kHz audio band.

Finally, Figure 9 shows the full signal chain, from ADC input to DAC output, with the DSP running the same Dolby® Pro Logic® IIx + Dolby Headphone® 2 algorithm. Small coupling artifacts are present in the noise floor, but are all below the -125 dB level. Dynamic Range performance for the entire signal chain across the 20 Hz - 20 kHz audio band is 107 dB (A-weighted).

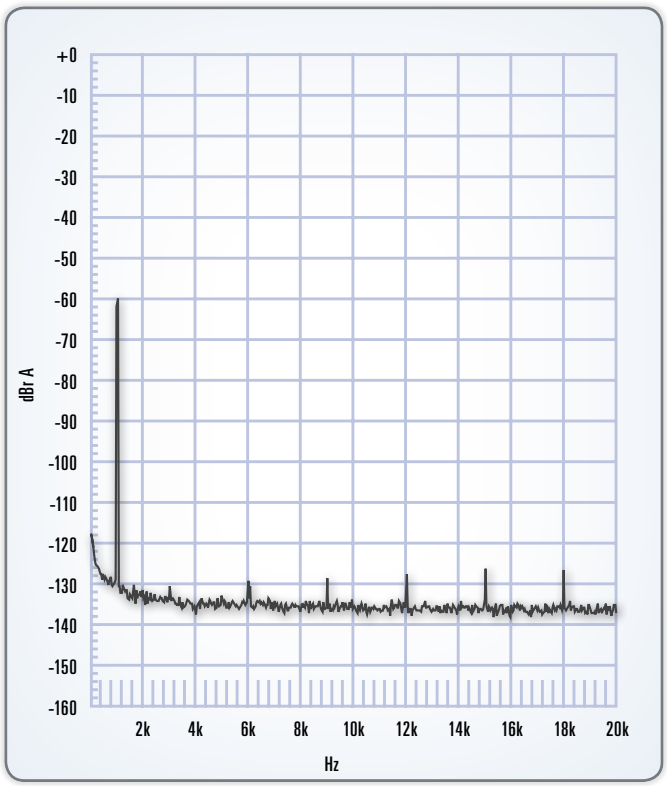

Figure 9. Analog-In To Analog-Out Performance at -60dB Input Level with DSP Enabled

CONCLUSION

A new continuous-time converter architecture has been demonstrated which addresses the shortcomings of a traditional switched-capacitor converter when used in a noisy digital environment. These converters are remarkably immune to interference from a high-performance DSP. These converter architectures open up numerous new markets where manufacturers seek even higher levels of integration in their systems, along with complex post-processing and decoding, without sacrificing analog performance.

[1] David A. Johns and Ken Martin, Analog Integrated Circuit Design (New York: John Wiley & Sons, 1997), p. 543. [2] United States Patent No. 4,746,899. [3] United States Patent No. 7,382,300.