KEY DESIGN CONSIDERATIONS FOR HIGH QUALITY AUDIO ADC PERFORMANCE

Duncan Macadie
Technical Marketing Engineer

ABSTRACT
The design of sigma-delta audio ADCs requires a balancing act between design issues such as the resolution and order of the device, and commercial considerations including cost and size. The crucial concern in all of this is the performance of the ADC. This paper examines the key design variables in the implementation of sigma-delta modulator ADCs and discusses their effect on performance, focussing on the range of sigma-delta audio ADCs from Wolfson Microelectronics plc.

INTRODUCTION
Sigma-delta modulator (SDM) based Analogue to Digital and Digital to Analogue Converters (ADCs and DACs) have been available for some time in audio systems, and are now common in a wide range of applications from DVD recorders to MP3 players and digital cameras. The performance benefits of the sigma-delta-based ADC for audio applications, versus other conversion topologies such as successive approximation or flash, are based on two principles; oversampling, and noise shaping.

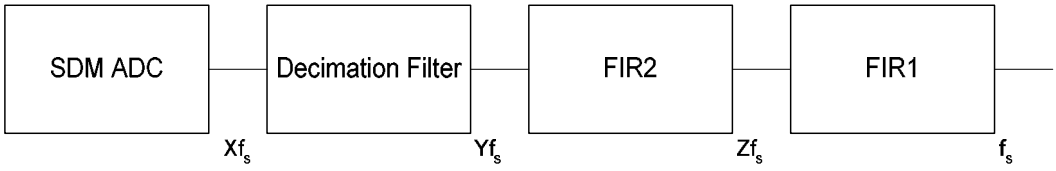
The audio signal is sampled within the sigma-delta modulator at a rate significantly higher than the Nyquist frequency. This spreads the quantisation noise inherent to the digitisation process over a wide frequency band, so that less of the noise is present in the audio frequency bandwidth.

The sigma-delta modulator also acts as a low-pass filter for the signal and a high-pass filter for the noise, shaping the noise such that a high proportion of the noise energy is contained above the audio signal bandwidth. The oversampled data is then filtered and decimated to remove the quantisation noise and lower the data rate from the oversampled rate to the Nyquist rate, whilst eliminating signal frequency components with the potential to alias into the audio band.

The application of these two principles in Wolfson's sigma-delta audio ADCs result in systems which are capable of recording a huge dynamic range of audio input, such that when the sound is eventually re-played, the user can have the same listening experience as those present at the original recording.

AUDIO ADC ARCHITECTURE AND OPERATION

A high-level block diagram of an audio ADC is shown below.



SDM: Sigma-Delta Modulator
ADC: Analogue to Digital Converter
FIR: Finite Impulse Response filter

Figure 1: Sigma-Delta-Based Audio ADC

The ADC is comprised of a number of stages, the main body of which is the sigma-delta modulator ADC. There are a number of ways in which the sigma-delta modulator can be constructed, the key architectural variables being the order, resolution and topology of the ADC. Changing any of these affects the performance, stability, size and cost of the device. Wolfson Microelectronics plc have carefully balanced these variables in order to produce ADCs which process sound brilliantly, whilst also meeting customers' cost and board area budgets.

First order sigma-delta modulators are inherently stable. However, their out of band noise performance is relatively poor, and significant benefits can, in theory, be gained by designing higher order modulators. Hypothetically, the higher the order of the modulator, the greater the SNR for a given oversampling ratio (OSR). Additionally, higher order modulators provide significant improvements in dynamic range performance and reduction of idle pattern tones.

Unfortunately, in practice, single-loop modulators of 3rd order or higher are only conditionally stable. Such circuits are more sensitive to component matching than low-order SDMs, and their gain must be limited to prevent the SDM entering a state of large amplitude/low frequency oscillation, a condition that is unacceptable for even the shortest period of time in audio applications. It is possible to prevent the SDM from becoming unstable by choosing appropriate gain coefficients and restricting the range of operation of the device. Achieving this stability can be complex and costly. A balance must therefore be struck between the improved performance of the high-order modulator and the stability and relative simplicity of the low-order modulator.

The resolution of the ADC quantiser is a key issue; each additional bit of resolution provides a decrease in quantisation noise, and therefore an improvement in SNR. This comes at the cost of a doubling in circuit size for each extra bit, and a subsequent increase in power consumption and cost. Early sigma-delta ADCs were primarily designed with 1-bit quantisers, which have the advantage of being inherently linear, and are relatively simple and cheap to implement. The use of a 1-bit quantiser allows the inclusion of a 1-bit DAC in the SDM feedback path, also inherently linear, whereas a multi-bit DAC has the potential to introduce non-linearities into the audio ADC.

As SDM designs have evolved the advantages of multi-bit quantisation, chiefly the increase in SNR of 6dB for every extra bit of resolution, have outweighed the drawbacks of more complex designs. Wolfson's high performance ADC range are multi-bit in design, and any potential non-linearities that could be introduced by the DAC, which manifest as harmonic or inter-modulation distortion, are minimised by a Dynamic Element Matching (DEM) scheme in the feedback path.

SDM ADC architectures are based on two topologies - single loop, and cascade or MASH (multi-stage noise-shaping). Within these categories, designers have many options available to them in determining the architecture of the circuit, each with advantages and disadvantages.

In the single loop case, the ADC has a single quantiser, and the order of the modulator is determined by the number of integrators within the loop. While there may be a number of internal loops within the ADC, there is a single data path from input to output. Such designs are relatively simple to implement, and are robust in their insensitivity to component matching.

In the cascaded topology, there are a number of stages to the modulator, typically of different order and resolution, which are combined at the output. The cascaded architecture has a number of advantages over the single-loop model, including:

Stability - the overall order of the modulator is the sum of the orders of all the stages, thus a number of low-order stages can be combined into a higher-order modulator, without making the system unstable.

Resolution - the resolution of the modulator is the sum of the resolutions of all the stages, therefore it is possible to construct a high-resolution ADC without having to design a prohibitively large and costly single circuit.

Noise cancelling - the error signal from the first stage of the cascaded modulator is fed to the second stage, processed, then used to cancel the noise from the first stage upon recombination at the output.

Performance - the combination of the above factors produces a less complicated ADC with significantly better performance than an equivalent single-loop design.

Sigma-delta ADCs from Wolfson Microelectronics plc are designed in a cascaded configuration, with loop gain coefficients carefully chosen to maximise the output SNR of the device. Dither, or noise with a specified probability density function, is added in the ADC to eliminate idle tones, improving the quality of the output further.

The next stage in the audio ADC is the decimation filter, which carries out a number of tasks. Firstly, the decimation filter removes the shaped quantisation noise introduced during the SDM process. The decimation filter also reduces the data rate of the signal from the oversampled rate of the SDM to the Nyquist rate for compatibility with standard audio rates. Finally, the decimation filter prevents aliasing of the original signal during the decimation process. This is necessary as it is likely that the analogue pre-ADC filter will have a gradual roll-off, which will not have removed all frequency components out with the audio bandwidth. When the signal is oversampled, these frequency components are of no concern, but when the signal is decimated in the digital domain, the filter must ensure that the components are not aliased back into the audible frequency bandwidth.

Although decimation filtering can be carried out in a single stage, Wolfson ADCs are implemented with several stages of decimation and filtering. This is the most effective and economic way of removing both the out of band quantisation noise introduced by the SDM and the components of the original signal which could potentially be aliased into the audio bandwidth.

With this architecture, it has been possible for Wolfson Microelectronics plc to implement multi-bit, low-order sigma-delta ADCs which display excellent audio capture performance in applications such as DVD recorders, exhibiting a dynamic range in excess of 110dB with sampling rates from 8kHz to 192kHz. This level of performance is illustrated in Figure 2.

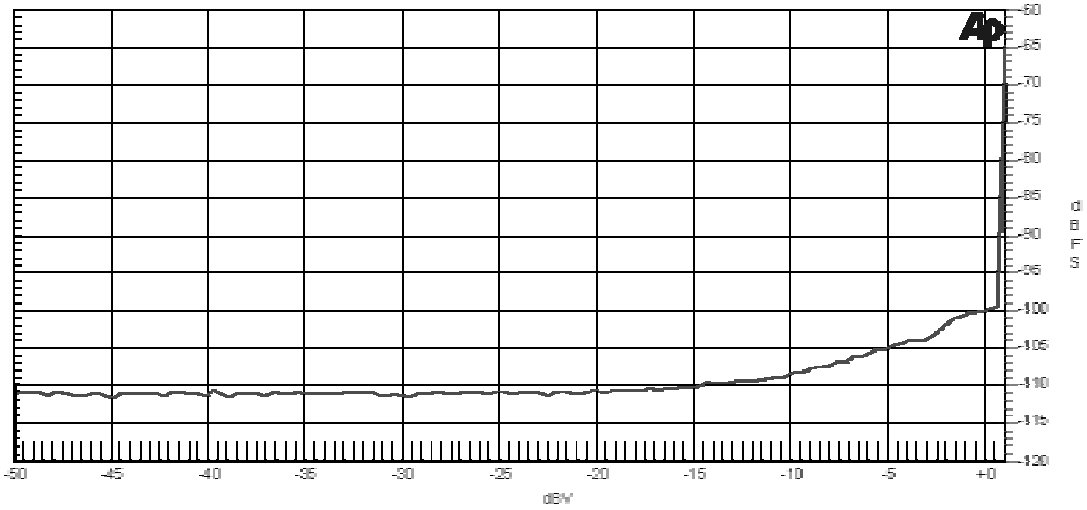


Figure 2: Wolfson Audio ADC: THD+N at f_s = 48kHz

SUMMARY

Wolfson Microelectronics plc recognises that while their customers want excellent performance under laboratory conditions, end-customers want high quality audio capture and playback in their homes, offices and on the move, from their DVD recorders, hi-fi systems and mobile phones. Wolfson's continuing success in these markets is in no small part due to their focus on the quality of the end-customer's audio experience.

To that end, audio ADCs from Wolfson Microelectronics plc are implemented in a low-order, multi-bit, cascaded sigma-delta based architecture. The low order sigma-delta modulator is stable, allowing the ADC to cope with the demands placed upon it by the wide range of audio inputs applied to the device. The multi-bit quantiser and cascaded topology maximises the SNR performance of the ADC, enabling the devices in which they are incorporated to capture the maximum range of audio inputs. This architecture results in ADCs which exhibit excellent performance in a wide range of audio applications.